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On modeling and control of Multilevel Converters and PLL algorithms

Tesis que presenta

Misael Francisco Martínez Montejano

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En la opción de

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Director de la Tesis:

Dr. Gerardo Escobar Valderrama

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On modeling and control of multilevel converters and PLL algorithms

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On modeling and control of multilevel converters and PLL algorithms

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To my parents with love

Summary

The present thesis is focuses in the study of the multilevel converters and the the phase-locked loop algorithms.

In the first five chapters, two of the main topologies of multilevel converters are studied, namely, diode clamped multilevel converter (NPC) and cascaded H-bridge multilevel converter (HB). First, a model is obtained that described the dynamics of the three level NPC converter used in a synchronous rectifier application. The highly nonlinear model, originally in abc-coordinates, is also expressed in its $\alpha\beta\gamma$-coordinates. Special attention is given to the γ-component of the control input, which represents a degree of freedom crucial for the balancing of the capacitors voltages. Then, based on this model, it is presented an adaptive controller that guarantees regulation and balance of the output capacitors voltages, as well as a close to unity power factor. Next, the modeling and the control design processes are presented for a cascade H-bridge single-phase multilevel converter used as a shunt active filter. Crucial for the developments is the transformation of the model in terms of the sum and the difference of the squares of the capacitors voltages. Moreover, it is shown that, while the current tracking problem and the regulation problem depend on the sum of the injected voltages, the balance depends on the difference between them. It is also presented a controller for the cascade H-bridge three-phase multilevel converter used as a shunt active filter. Based on the proposed mathematical model, the controller is designed to compensate harmonic distortion and reactive power due to a nonlinear distorting load. Simultaneously, the controller guarantees regulation and balance of all capacitor voltages. The idea behind the controller is to allow distortion of the current reference during the transients to guarantee regulation and balance of the capacitors voltages.

The chapters 6 and 7 of the thesis deals with the design of phase-locked loop (PLL) algorithms. Although PLLs have been widely used in many electronic applications, the PLL presented here is of special interest in the synchronization of power electronic equipment coupled with the electric network. In particular, the presented PLL has been designed to work in fixed reference frame coordinates, and thus the proposed algorithm is referred as fixed reference frame PLL (FRF-PLL). The scheme provides an estimation of the angular frequency, and both the positive and negative sequences of the fundamental component of a three-phase signal. The design of the FRF-PLL is based on a complete description of the source voltage involving both positive and negative sequences in stationary coordinates and considering that the angular frequency is uncertain. Therefore the proposed scheme is of special interest in cases of unbalanced operation. Also, a simpler scheme is presented for the balanced case. Finally, the design and implementation of a single-phase PLL based on an adaptive observer is also presented. This algorithm assumes that the signal is produced by a harmonic oscillator where the frequency is an unknown parameter, and only one of the

states is available. In contrast to many PLL schemes, the proposed scheme does not rely in the usual assumption of linearity around the desired equilibrium point, which leads to local results.

Contents

Notation

Frequent Acronyms

AC	alternating current.
BIBO	bounded input bounded output.
BBD	bucket brigade delay.
DC	direct current.
DC-DC	direct current to direct current.
EMI	electro magnetic interference.
DSP	digital signal processor.
ESR	equivalent series resistances.
FFT	fast Fourier transform.
HR	harmonic reducer.
IC	integrated circuit.
IGBT	isolated gate bipolar transistor.
LPF	low pass filter.
LTI	linear time invariant.
MOSFET	metal-oxide-semiconductor field-effect transistor.
PCC	point of common connection.
PF	power factor.
PFC	power factor correctors or unit power factor converter.
PI	proportional integral.
PIS	synchronous proportional integral.
PWM	pulse width modulation.
SPWM	sine pulse width modulation.
RHS	right hand side.
RMS	root mean square.
THD	total harmonic distortion.
VSI	voltage source inverter.

Most common mathematical symbols

$\mathbb{R}$	field of real numbers.
$\mathbb{C}$	field of complex numbers.
$\mathbb{R}_{-}^{m\times n}$ or $\mathbb{R}_{-}$	set of all proper and real rational stable transfer matrices.
$\mathbb{R}^n$	linear space of ordered n-tuples in $\mathbb{R}$.
$\in$	"belong to".
$\stackrel{\triangle}{=}$	"defined as".
$(\cdot)^\top$	transpose operator.
$(\cdot)^{-1}$	inverse operator.
$\bar{\sigma}(.)$	largest singular value of the matrix.
$Re(\alpha)$	the real part of $\alpha \in \mathbb{C}$.
$\mathscr{L}^{-1}$	inverse Laplace transform.
$\|A\|_\infty$	induced ∞-norm of a matrix A.
$\mathcal{L}_2$	space of square integrable functions.
$\mathcal{L}_\infty$	space of bounded functions.
$\mathcal{H}_\infty$	set of $\mathcal{L}_\infty$ analytic in $Re(s) > 0$.
prefix $\mathcal{R}$	real rational, e.g., $\mathcal{RH}_\infty$, $\mathcal{RH}_\in$.
t	time, $t \in \mathbb{R}_{\geq 0}$.
$\frac{d}{dt}(\cdot), \dot{(\cdot)}$	differentiation operator.
$(\cdot)_k^p$,	k-th harmonic coefficients for the positive sequence representation.
$(\cdot)_k^n$	k-th harmonic coefficients for the negative sequence representation.
I_n	identity matrix of dimension n.
$\mathcal{J}$	skew symmetric matrix $\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$
$e^{(\cdot)}$	exponential function
$\mathcal{H}$	set of indexes of the considered harmonic components
$\rho(\cdot)$	rotation vector defined as $\begin{bmatrix} \cos(\cdot) \\ \sin(\cdot) \end{bmatrix}$.
$\hat{(\cdot)}$	estimate of $(\cdot)$.
$\tilde{(\cdot)}$	error between a quantity and its reference.
	$(\cdot) - (\cdot)^*$, $\hat{(\cdot)} - (\cdot)$.
$(\cdot)^*$	desired external references.

List of Figures

Chapter 1

Introduction

Since the emergence of the first semiconductor device, the evolution of electronics has become an unquestioned reality. It is evident that the development of electronic equipment has significantly changed patterns of behavior of individuals and has substantially improved the quality of life. The great challenge that Electrical Engineering is facing at the beginning of this new millennium is to guarantee an operation of the power systems with the highest quality as demanded by different loads. To achieve this goal, the power electronics is playing an important role in the design and construction of equipment able to correct the distortions typical of a normal power system; thus improving the quality with which the Electricity is delivered to the load.

The important criterion, which makes the power electronics solutions unique, is that they are fundamentally multifunctionals, and can provide not only their main interfacing function, but also various utility functions. The general trend in power electronic devices has been to switch power semiconductors at increased frequencies to minimize harmonics and reduce passive component sizes. There are several areas in which power electronics plays a vital role. The research areas of power electronics include:

- ▷ Converters for utility applications such as static var compensation, voltage sag support, HVDC distribution systems, large variable speed drives.
- ▷ Interfacing with distributed energy resources such as micro turbines, fuel cells, and solar cells.
- ▷ Harmonics,power quality, and power filter design.
- ▷ Hybrid electric vehicle (HEV) applications such as motor drives or dc-dc converters.
- ▷ Soft switching inverters and DC-DC converters.
- ▷ Areas like transportation and utility applications.

The points mentioned above constitute a challenge in the field of power electronics, and had contributed to the emergence of new semiconductor devices, new switching and control strategies, and new topologies.

In the last decades the pulse width modulated two-level converters have been the dominant topology in the low power and some selected medium power applications. There has

been on-going research on these power converters and, as technology evolves and matures, various new trends and performance of power converters can be identified. Several important issues play a key role in these new trends. Factors like increasing the power density, improving performance, reducing the cost, and also increasing the VA ratings of the converter are considered. There are several ways in which these factors can be achieved, for instance, to increase the power density the switching losses must be reduced. This is obtained by using soft-switching techniques, efficient power devices, and improving the thermal management. Now, to increase the system performance, then it is required to reduce the total harmonic distortions, to reduce the EMI problems, and to improve the dynamic response of the system.

As the power demand continues to grow unceasingly, the converters power ratings should also increase. In case that the conventional two-level converters are used in these high power applications, then the rating of the devices has to increase considerably, that is, the blocking voltage rating, current rating, thermal management, and so on must be increased accordingly. Multilevel converters, in contrast, allow high power ratings of the converters but using low rating devices. Recently, the study of multilevel converters has become an attractive solution in medium and high power applications as the voltage stress of power semiconductors, voltage harmonics, and electromagnetic interferences can be reduced. One of the first topologies of multilevel converters was the neutral point clamped inverter topology proposed by Nabae et al. in 1981. These converters incorporate a topological structure that allows a desired output voltage to be synthesized from among a set of different voltage sources isolated or interconnected. Thus, by synthesizing the AC output voltage from several DC voltage levels, staircase waveforms are produced, which approach the sinusoidal waveform with low harmonic distortion, as shown in Fig. 1.1. Thanks to the reduction of low frequency harmonics from the AC voltage, the size of the AC inductances can be reduced as well. In addition, they allow to handle at least twice the voltage of a conventional converter, while using the same type of switching devices; that is, due to the series connection of semiconductors, it is possible to reach medium-high voltages with standard components. The multilevel converter can therefore be described as a voltage synthesizer.

Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is

$$k = 2m + 1 \tag{1.1}$$

and the number of steps p in the phase voltage of a three-phase load in wye connection is

$$p = 2k - 1 \tag{1.2}$$

There are several advantages of multilevel inverters such as

- ▷ Low manufacturing costs as low rating devices are used;
- ▷ Improved waveform quality as levels in the converter are increased;
- ▷ Compact modules and no transformer needed;

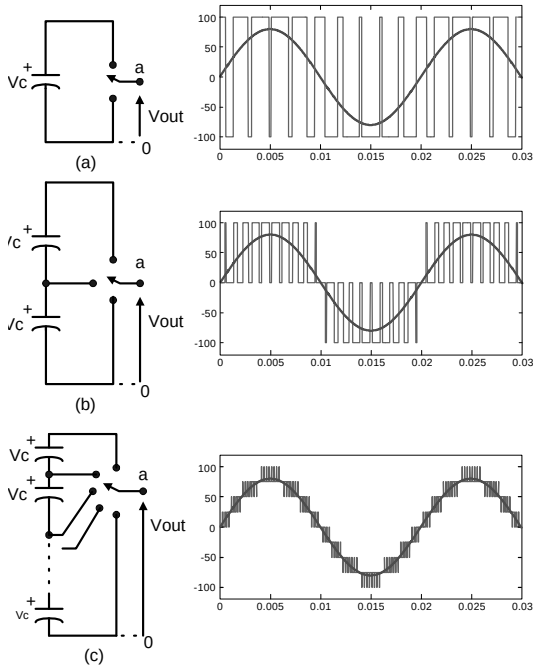

Figure 1.1: Synthesis of the output voltage in multilevel converters: **a)** two levels, **b)** three levels and **c)** n-levels.

- ▷ Better synthesizing of the output waveforms which reduces the output filters and the rating of the passive components;
- ▷ Many possible connections are available such as single-phase, three-phase, and multi phase connections;
- ▷ Low switching frequency yields high efficiency.

When series connected capacitors are used to divide the DC-link voltage, three-level inverters (multilevel converters in general) have a DC-link voltage problem due to the following reasons:

- ▷ Unequal capacitor values due to manufacture tolerances.
- ▷ Unequal loading of the capacitors due to unintended switching delays.
- ▷ Unequal loading of the capacitors due to nonlinear loads containing even order harmonics.
- ▷ Dead-time implementation, which is always necessary in voltage source converters.
- ▷ Transformer-secondary leakage inductance or voltage imbalance due to manufacturing tolerances.
- ▷ Unbalanced load due to imbalances between the phases of the three-phase load.

- ▷ Dynamic operating conditions such as acceleration or deceleration of a motor.
- ▷ Imbalances in the parameters of the power semiconductors switching devices.

The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers. This makes these unique power electronics topologies suitable for flexible AC transmission systems (FACTS) and custom power applications. The use of a multilevel converter to control the frequency, voltage output, phase angle, and active and reactive power flow at a DC/AC interface provides significant opportunities in the control of distributed power systems.

Additional applications of multilevel converters include adjustable speed motor drives, static var compensation, dynamic voltage restoration, harmonic filtering; or for a high voltage DC backtoback converter. As distributed power sources are expected to become increasingly prevalent in the near future, the use of a multilevel converter to control the frequency and voltage output (including phase angle) from renewable energy sources will provide significant advantages because of its fast response and autonomous control. Additionally, multilevel converters can also control the active and reactive power flow from a renewable energy source connected to the utility. If a capacitance is connected in parallel to the renewable energy source, then a multilevel converter can provide static var compensation even when there is no output power from the photovoltaic or fuel cell energy source. If banks of batteries or large capacitors are on the DC bus, then a multilevel converter can provide significant ridethrough capability for voltage sags or load swings experienced at the utility interface connection.

Multilevel inverters can operate not only with PWM techniques but also with amplitude modulation (AM), improving significantly the quality of the output voltage waveform. With the use of amplitude modulation, low frequency voltage harmonics are perfectly eliminated, generating almost perfect sinusoidal waveforms, with a THD lower than five percent. Another important characteristic is that each device can be operated at a low switching frequency, reducing the semiconductor stresses, and therefore reducing the switching losses.

1.1 Topologies of multilevel converters

Up to now, the topologies for high power multilevel converter are classified in three main types: flying capacitor converter (FC), diode clamped converter (NPC) and cascaded H-bridge converter (HB).

A three-level diode-clamped inverter (NPC) is shown in Fig.1.2. In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, $C1$ and $C2$. The middle point of the two capacitors n can be defined as the neutral point. The output voltage has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S1$ and $S2$ need to be turned on while the rest is maintained off; for $-V_{dc}/2$, switches $S3$ and $S4$ need to be turned on; and for the 0 level, $S2$ and $S3$ need to be turned on. The key components that distinguish this circuit from a conventional two-level inverter are diodes $D1$ and $D2$. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both $S1$ and $S2$ turn on, the voltage across a and 0 is V_{dc}, i.e., $v_{a0} = V_{dc}$. In this case, $D2$ balances out the voltage sharing between $S3$ and $S4$ with $S3$ blocking the voltage across $C1$

and $S4$ blocking the voltage across $C2$. Notice that output voltage v_{aN} is ac, and v_{a0} is dc. The difference between v_{aN} and v_{a0} is the voltage across $C2$, which is $V_{dc}/2$. If the output is removed out between a and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0.

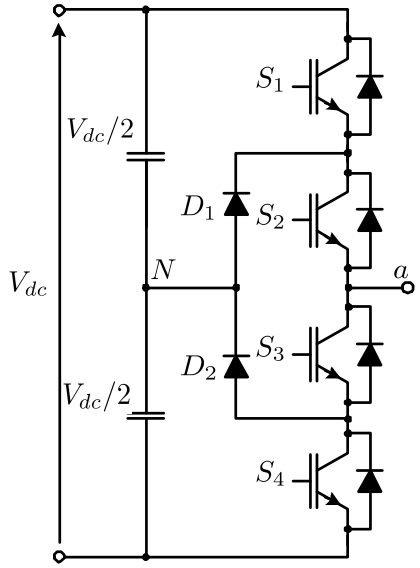

Figure 1.2: Neutral Point Clamped (NPC) multilevel converter.

Figure 1.3 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter (FC). The circuit has been called the flying capacitor inverter [1], [5], [6] with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig.1.3 provides a three-level output across a and N, i.e., $v_{aN} = V_{dc}/2$, 0, or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S1$ and $S2$ need to be turned on; for $-V_{dc}/2$, switches $S3$ and $S4$ need to be turned on; and for the 0 level, either pair $(S1, S3)$ or $(S2, S4)$ needs to be turned on. Clamping capacitor $C1$ is charged when $S1$ and $S3$ are turned on, and is discharged when $S2$ and $S4$ are turned on. The charge of $C1$ can be balanced by proper selection of the 0-level switch combination.

A different converter topology which is based on the series connection of single-phase H-bridge inverters (HB) with separate dc sources is shown in Fig.1.4. This figure shows the power circuit for one phase leg of a five-level inverter with two cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from $-2V_{dc}$ to $2V_{dc}$ with five levels, and the staircase waveform is nearly sinusoidal, even without filtering.

Other topologies can be found in the literature of power and industrial electronics, which are often a combination of the three basic topologies or modifications of them. They can be found under the following names:

- ▷ Asymmetric Hybrid Multilevel Cells.

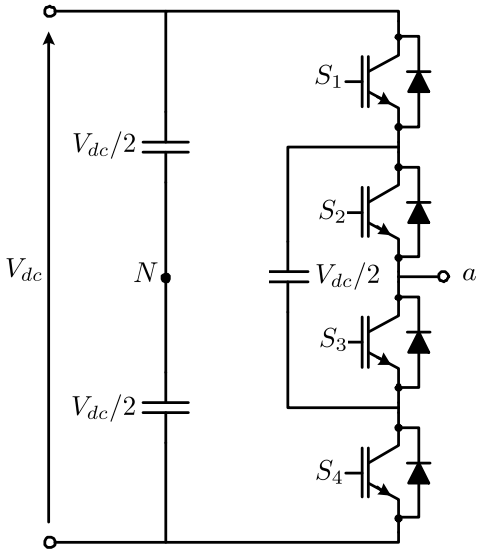

Figure 1.3: Flying capacitor (FC) multilevel converter.

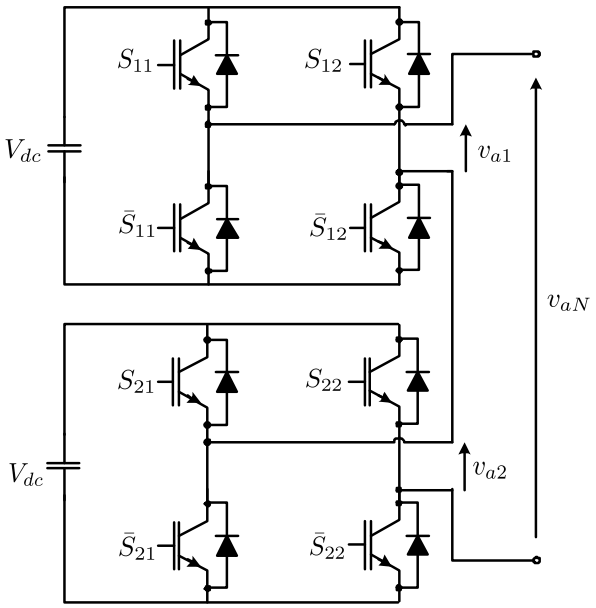

Figure 1.4: H-bridge (HB) multilevel converter.

- ▷ Mixed-Level Hybrid Multilevel Cells.
- ▷ Soft-Switched Multilevel Inverters.
- ▷ Matrix converters.
- ▷ Transformer-coupled inverters.
- ▷ Diode/capacitor clamped converters.
- ▷ New diode clamped multilevel converters.

1.2 Classification of Modulation Strategies

The modulation methods used in multilevel inverters can be classified according to switching frequency as fundamental switching frequency and high switching frequency PWM. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classical carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage [1], [2], [3]. Another interesting alternative is the SVM strategy, which has been used in three-level inverters [4].

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination [5], [6] and the space-vector control (SVC) [7]. Some of the most important modulation techniques are listed below:

- ▷ Multilevel SPWM. Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals [2], [8], [9].
- ▷ SVM technique. It can be easily extended to all multilevel inverters [10]-[16]. These vector diagrams are universal regardless of the type of multilevel inverter. In other words, the modulation is valid for five-level diode-clamped, capacitor-clamped, or cascaded inverter. Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. However, as the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically.
- ▷ Selective Harmonic Elimination. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $m-1$ harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits.

- ▷ SVC. A conceptually different control method for multilevel inverters, based on the space-vector theory, has been introduced [17]. This control strategy, called SVC, works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of SVM. The main idea in SVC is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector. This method is simple and attractive for high number of levels. As the number of levels decreases, the error in terms of the generated vectors with respect to the reference will be higher; this will increase the load current ripple.

- ▷ Direct Torque Control (DTC). This technique has been developed for low-voltage two level inverters as an alternative to the field oriented method to effectively control torque and flux in AC drives [18]. DTC and hysteresis current control techniques have also been applied in multilevel inverters [19]. It must be noticed that one major manufacturer has been selling medium-voltage three-level diode clamped inverters controlled with DTC [20].

1.3 Phase locked-loop algorithms

One crucial aspect in the control of grid-connected power converters, is the detection of the fundamental-frequency positive-sequence component of the utility voltage under unbalanced and distorted conditions. Specifically, the detection of the positive-sequence voltage component at fundamental frequency is essential for the control of distributed generation and storage systems, flexible AC transmission systems (FACTS), power line conditioners and uninterruptible power supplies (UPS). The most widely accepted solution to provided this synchronization are the phase-locked loop (PLL) based technics. The basic PLL concept has been known and widely utilized since it was first proposed in 1922. From that time, PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth.

A phase-locked loop (PLL) is a system that generates an alternating signal whose phase shift and frequency are equal to those of a "reference" signal. In general, a conventional PLL comprises a phase frequency detector (PFD) aimed to detect phase error and frequency error between the sensed input signal and an internally reconstructed signal. This error signal is processed in a filter and the result is used to adjust the frequency of a voltage controlled oscillator (VCO). A PLL circuit responds to both the frequency and the phase shift of the input signal. It may automatically increase or decrease the frequency of a controlled oscillator until its output signal matches both frequency and phase shift of the reference. The PLL scheme compares its output phase with the phase of an incoming reference signal and adjusts itself until both are aligned, i.e., the PLL output's phase is "locked" to that of the input reference. Once the loop is locked (the phase difference between the output and the input signals is very close to zero) the frequency of the output signal is a multiple (integer or fractional) of the input signal's frequency.

One of the most common implementations of integrated circuits' PLLs is in frequency synthesizers, where PLLs are used to generate a set of programmable frequencies. Applications of frequency synthesizers include LO (Local Oscillator) for up- and down- conversion in wireless communications systems (such as cell phones), demodulation of both FM and

AM signals, recovery of clock timing information in a data stream (such as those made available in a disk drive), and clock multipliers in microprocessors. In wireless communications ICs, PLLs have to achieve key performance metrics of various parameters, including phase noise, spur levels, and lock time, which tend to trade off with each other and hence challenge IC designers everywhere. Given the widespread use of PLLs and their complexity, a lot of research effort has been applied to the understanding of PLLs and simulation techniques that can facilitate their implementation in ICs.

One crucial aspect in the control of grid-connected power converters is the detection of the fundamental-frequency under distorted conditions. In particular, in three-phase systems, it is necessary to detect the positive-sequence component of the utility voltage under unbalanced and distorted conditions. The PLL schemes have been used in power electronics systems which require grid voltage information, such as the frequency, phase angle and amplitude. They are in fact the most widely accepted solution to provide synchronization with the grid. The detection and synchronization to the fundamental component is essential for the control of distributed generation and storage systems, flexible ac transmission systems (FACTS), power line conditioners and uninterruptible power supplies (UPS).

1.4 Objectives, structure and main contributions

The objectives of this thesis can be summarized as follows:

[First]: to establish mathematical models based on differential equations for the different topologies of multilevel converters. The hypothesis is that with a correct description of the dynamics of the systems, is possible to design a control law that would maximize the characteristics of the system under study.

[Second]: based on the mathematical models proposed, design an appropriated control law in order to obtain the most benefits of the systems. The main reason of design the control law in base of the model is try to identify the control input (or inputs) that permits the balance of the capacitor voltages, which is the most important problem with the multilevel converter systems.

[Third]: validate the mathematical models and the control laws with simulations results and/or experimental results.

[Fourth]: demonstrate that with a complete description of the source voltage, is possible to design a PLL algorithm to perform properly under unbalanced conditions, and to be robust against angular frequency variations, also robust against harmonic distortion present in the source voltage signal.

[Fifth]: validate the proposed PLL algorithms with simulation results and/or experimental results.

The thesis is structured as follows:

Chapter 2 presents a model describing the dynamics of a three level neutral point clamped converter used in a synchronous rectifier application. The highly nonlinear model, originally in abc-coordinates, is also expressed in its $\alpha\beta\gamma$-coordinates. Special attention is given to the γ-component of the control input, which represents a degree of freedom crucial for the balancing of the capacitors voltages.

Unlike others models presented in the literature [71], [75] that are more analytical models

describing the basic operation of the converter or the effects of the systems parameters, the proposed model is an average model working with continuous signals. This is true if the switching frequency is much faster than the nominal frequency, in this case, 50 or 60 Hz; then considering systems working with a switching frequency of 10 KHz, the assumption is correct. This means that the inputs of the model are the duty ratios instead of the switching sequence. Moreover, the proposed model is presented in $\alpha\beta\gamma$-coordinates, or fixed reference frame, instead of the rotating reference frame by using a combination of Clarke's and Park's transformations [73], [74], this is traduced in a minor computational requirements, and also, it is not required the knowledged of the angular frequency for the calculation of the reactive power and the instant power. It is also important to clarify that the proposed model represents the dynamics of the converter and is not an study with design purpose of the parameters of the converter [76]. The parameters of the converter are expressed in the model, but there are considered as an unknown constants.

Chapter 3 presents an adaptive controller for a synchronous rectifier using a three level NPC. The controller guarantees regulation and balance of the output capacitors voltages, as well as a close to unity power factor, simultaneously. The design is based on the model in $\alpha\beta\gamma$-coordinates of the three level converter above proposed. Special attention is given to the γ-component of the control input, since it has direct influence in the balancing of the capacitors voltages, represented here as the arithmetic difference of voltages.

Unlike other techniques of control [4], [72], [70], where are focused in obtaining the best switching sequence to solve the problems of balancing the voltages of the capacitors and harmonic elimination, based in analytical models, the proposed controller is based in a mathematical model, in this case, an average continuous model. This allow to obtain the proper duty ratios for the switching sequence and for the implementation it is necessary a correct modulation scheme, in this case it was implemented the proposed in [24].

Chapter 4 presents the modeling and control process of the cascade h-bridge single-phase multilevel converter used as an active filter. Based on the model, a controller is proposed to guarantee a current tracking of the line current towards a reference proportional to the line voltage. Simultaneously, the controller guarantees the regulations and balance of the capacitor voltages.

Chapter 5 presents the modeling and control process of the cascade H-bridge three-phase multilevel converter used as a shunt active filter. Based on the model, a controller is proposed to compensate harmonic distortion and reactive power due to a nonlinear load. Simultaneously, the controller guarantees the regulations and balance of the capacitor voltages. The results are shown for a cascade H-bridge three-phase five-level converter, however, all results can be easily extended to higher levels.

Chapter 6 presents the design and implementation of a single phase PLL based on an adaptive observer. The algorithm assumes that the signal is produced by a harmonic oscillator where the frequency is an unknown parameter, and only one of the states is available. A prototype has been built and experimental results are presented to asses its performance.

Chapter 7 presents a PLL which is able to provide an estimation of the angular frequency, and both the positive and negative sequences of the fundamental component of a three-phase signal. These sequences are provided in fixed reference frame coordinates, and thus the proposed algorithm is referred as fixed reference frame PLL (FRF-PLL). The FRF-PLL is intended to perform properly under severe unbalanced conditions, and to be robust against

angular frequency variations in the three-phase source voltage signal. Although not considered in the design, it is shown that the scheme is also robust against harmonic distortion present in the source voltage signal.

Finally, the concluding remarks, the scientific production and the future work.

Chapter 2

NPC Multilevel Converter: Mathematical Model

2.1 Introduction

Among the various multilevel converters, the NPC or Diode-Clamped topology is undoubtedly one of the most used and studied.

The advantages of the NPC topology are:

- ▷ The lock voltage of one semiconductor device is a single voltage input of one capacitor, $V_{pn}/(n-1)$ in the case of n levels.
- ▷ The number of capacitors required is small compared with other multilevel topologies. This point is especially interesting since they are components reagents which entail a higher cost in the converter.
- ▷ Can be connected directly to a DC bus, without adding other additional capacitors.
- ▷ Does not require transformers.
- ▷ Change from one state to another via actuation of a single switch.

This topology presents, however, the followings drawbacks:

- ▷ The fixing diodes or clamping diodes must be chosen capable to driving the nominal current of the converter. This requirement must be considered seriously in the design of the converter.
- ▷ In topologies with more than three levels, it is required that the clamping diodes block different voltages depending on their position in the converter.
- ▷ It is necessary that the tensions of the capacitors remain balanced in any point of work, complicating the control system of the converter. The balancing of the voltages of capacitors is difficult as it is increasing the number of levels of the converter, it can even be impossible in some operating conditions.

In general, the provided advantages of NPC converters make interesting the task to develop a complete mathematical model of the converter in order to allow the design of more adequate control strategies.

This chapter presents a model that describes the dynamics of a three level neutral point clamped converter used in a synchronous rectifier application. The highly nonlinear model, originally in abc-coordinates, is also expressed in its $\alpha\beta\gamma$-coordinates. Special attention is given to the γ-component of the control input, which represents a degree of freedom crucial for the balancing of the capacitors voltages. It is shown that the arithmetic difference and sum of the capacitors voltages are two natural states of the system and, indeed, they reduce considerably the model expressions. It is also shown that the controller γ-component has a minimum influence on the sum of the capacitors voltages, but it has a strong influence on the difference, hence its importance in the capacitor voltage balance. Simulations are presented to validate the proposed model.

2.2 Model of the three level NPC inverter

The basic setup for the synchronous rectifier application using a three level NPC inverter discussed in this chapter is shown in Fig. 2.1, and the equivalent circuit with ideal switches is shown in Fig. 2.2.

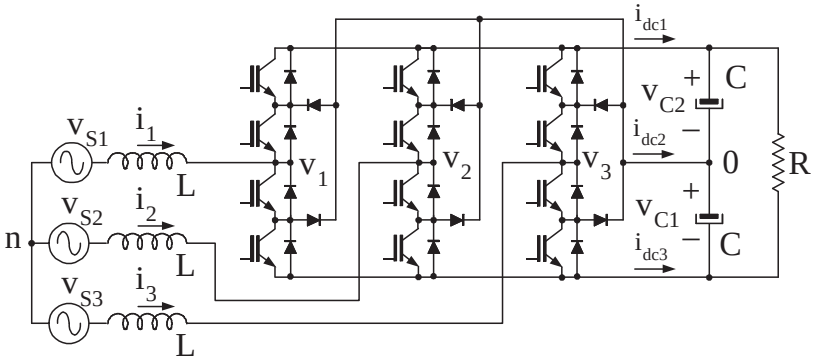

Figure 2.1: Synchronous rectifier based on a three level NPC inverter.

The modeling process is divided in two stages. In the first stage, we obtain the expressions for the inductor current dynamics, and second, we obtain the expressions to describe the dynamics of the capacitor voltages. Some approximations are proposed to reduce the complexity of such expressions. We note that a natural description of the capacitors voltages dynamics consists in considering, as controlled variables, the addition and the difference of both capacitors voltages. We conclude this section by presenting the transformation of the proposed model from abc-coordinates to $\alpha\beta\gamma$-coordinates where we introduce the third coordinate γ to consider the third degree of freedom available in the input control. This control component is crucial in the balancing of the capacitors voltages as it will become clear later.

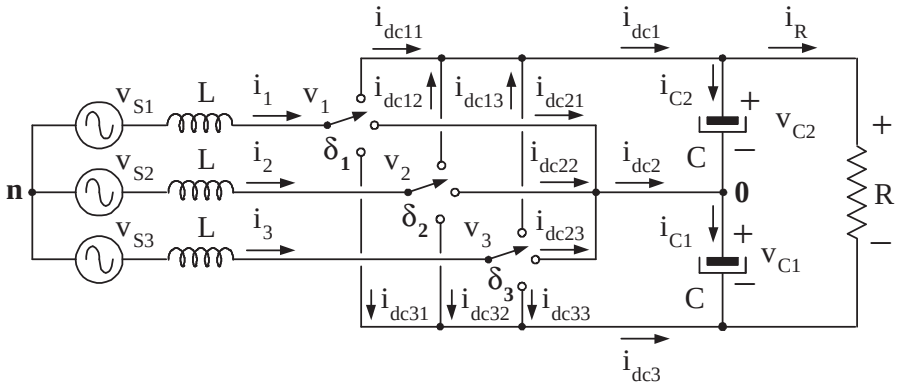

Figure 2.2: Synchronous rectifier equivalent circuit based on a three level inverter with ideal switches.

2.2.1 The inductors current dynamics

Direct application of Kirchhoff's Voltage Law (KVL) yields

$$\begin{aligned} v_{S1} &= L\frac{di_1}{dt} + v_1 + v_{0n} \\ v_{S2} &= L\frac{di_2}{dt} + v_2 + v_{0n} \\ v_{S3} &= L\frac{di_3}{dt} + v_3 + v_{0n} \end{aligned} \tag{2.1}$$

where

v_{S1}, v_{S2}, v_{S2}	:	source voltages referred to "n"
i_1, i_2, i_3	:	inductor currents
v_1, v_2, v_3	:	injected voltages referred to "0"
v_{0n}	:	voltage at "0" referred to "n"
L	:	inductance of input inductors
C	:	capacitance of output capacitors
R	:	load resistance
i_{dc1}, i_{dc2}, i_{dc3}	:	currents at top, middle and bottom connection points of capacitors
i_{C1}, i_{C2}	:	capacitors currents

Since source voltages are equilibrated and no fourth wire is considered in this application it can be assumed that

$$v_{S1} + v_{S2} + v_{S3} = 0 \ , \quad i_1 + i_2 + i_3 = 0$$

Adding all three equations (2.1), side by side, yields

$$v_{0n} = -\frac{1}{3}(v_1 + v_2 + v_3)$$

Direct substitution of v_{0n} in (2.1) yields

$$\begin{bmatrix} v_{S1} \\ v_{S2} \\ v_{S3} \end{bmatrix} = \begin{bmatrix} L\frac{di_1}{dt} \\ L\frac{di_2}{dt} \\ L\frac{di_3}{dt} \end{bmatrix} + \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{2.2}$$

The voltages in the switches $v_i\,(i \in \{1,2,3\})$ referred to "0" point are defined in terms of the switching positions δ_i as follows

$$v_i = \begin{cases} v_{C2} & , \quad \delta_i = 1 \\ 0 & , \quad \delta_i = 0 \\ -v_{C1} & , \quad \delta_i = -1 \end{cases} \quad , \quad i \in \{1,\,2,\,3\} \tag{2.3}$$

According to (2.3), three states are allowed, and an expression of v_i (for every $i \in \{1,\,2,\,3\}$) in function of δ_i can be obtained. A single quadratic function that fits all three states is

$$v_i = \left(\frac{v_{C2} - v_{C1}}{2}\right)\delta_i^2 + \left(\frac{v_{C2} + v_{C1}}{2}\right)\delta_i \tag{2.4}$$

where $\delta_i \in \{-1, 0, 1\}$.

Figure 2.3 shows the quadratic function used here to mimic the relationship (2.3) in the points of interest.

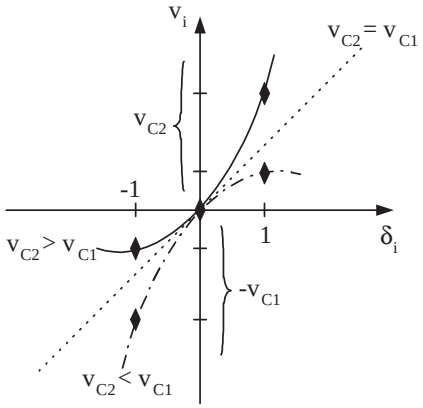

Figure 2.3: Description of the voltages functions v_i using a quadratic function of δ_i fitting all three points (♦), valid for each $i \in \{1,2,3\}$. For: **(–)** $v_{C_1} > v_{C_2}$, **(-·-)** $v_{C_1} < v_{C_2}$, and $(\cdots)$ $v_{C_1} = v_{C_2}$.

Notice also that, for a given v_i, v_{C1} and v_{C2}, there exists two roots for δ_i that solves eq. (2.4), however the following root is the only physically meaningful

$$\delta_i = \frac{-\frac{v_{C2}+v_{C1}}{2} + \sqrt{\left(\frac{v_{C2}+v_{C1}}{2}\right)^2 + 2(v_{C2} - v_{C1})v_i}}{v_{C2} - v_{C1}}$$

fulfilling the condition

$$-1 \leq \delta_i \leq 1$$

It is clear that $v_i \equiv 0 \iff \delta_i \equiv 0$. Moreover, for $v_{C1} \equiv v_{C2} \;\Rightarrow\; v_i = v_{C1}\delta_i$.

In conclusion the inductors currents dynamics can be modeled as (2.2) where the voltages v_i are computed as in (2.4).

Remark 2.1 Under the consideration that $v_{C2} \cong v_{C1}$ eq. (2.4) reduces to

$$v_i = \frac{v_{C2} + v_{C1}}{2}\delta_i \;\;, \quad i \in \{1,\, 2,\, 3\} \tag{2.5}$$

Thus, subsystem (2.2) can be approximated as

$$\begin{bmatrix} L\frac{di_1}{dt} \\ L\frac{di_2}{dt} \\ L\frac{di_3}{dt} \end{bmatrix} = -\frac{v_{C1} + v_{C2}}{6}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} + \begin{bmatrix} v_{S1} \\ v_{S2} \\ v_{S3} \end{bmatrix} \tag{2.6}$$

□

2.2.2 The capacitors voltages dynamics

Using Kirchhoff's Current Law (KCL) in the diagram of Fig.2.2 it is obtained the following relationships

$$\begin{aligned} i_{dc1} &= i_{C2} + i_R \\ i_{dc2} &= i_{C1} - i_{C2} \\ i_{dc3} &= -i_{C1} - i_R \\ 0 &= i_{dc1} + i_{dc2} + i_{dc3} \end{aligned}$$

where $i_{C1} = C\dot{v}_{C1}$, $i_{C2} = C\dot{v}_{C2}$, $i_R = (v_{C1} + v_{C2})/R$ and $i_{dci} = i_{dci1} + i_{dci2} + i_{dci3}$, for every $i \in \{1,\, 2,\, 3\}$.

From these expressions, the following relationships are obtained

$$i_{C2} + i_{C1} = i_{dc1} - i_{dc3} - 2i_R \tag{2.7}$$

$$i_{C1} - i_{C2} = i_{dc2} \tag{2.8}$$

Expressions for i_{dc1}, i_{dc2} and i_{dc3} are approximated as quadratic functions following a similar procedure as before.

A. Current i_{dc1}

First, it is established the relationship between each output current i_{dc1k} in terms of the three possible switch positions δ_k, and for every $k \in \{1, 2, 3\}$. Thus, for a given $k \in \{1, 2, 3\}$ three points are known, and a quadratic function relating i_{dc1k} and δ_k can be designed to fit all three points. Figure 2.4 shows the points and the fitting quadratic function for i_{dc1k} vs. δ_k which is valid for all $k \in \{1, 2, 3\}$.

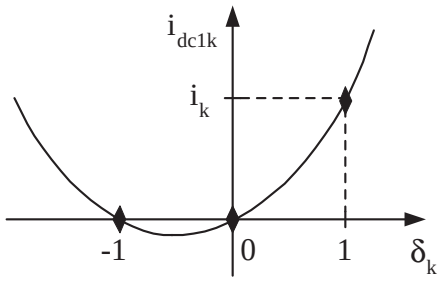

Figure 2.4: Description of the current functions i_{dc1k} using a quadratic function of δ_k, fitting all three points (♦), valid for each $k \in \{1, 2, 3\}$.

The expression for the k-th quadratic function is

$$i_{dc1,k} = (\delta_k + 1)\frac{\delta_k i_k}{2}$$

Now, since $i_{dc1} = \sum_{k\in\{1,2,3\}} i_{dc1k}$, we obtain the following expression

$$i_{dc1} = (\delta_1 + 1)\frac{\delta_1 i_1}{2} + (\delta_2 + 1)\frac{\delta_2 i_2}{2} + (\delta_3 + 1)\frac{\delta_3 i_3}{2} \tag{2.9}$$

B. Current i_{dc2}

Figure 2.5 shows the distribution of the three points (for each switch position) and the quadratic function fitting them. In this case the expression for the quadratic function relating current i_{dc2k} and δ_k is

$$i_{dc2k} = (1 - \delta_k^2)i_k$$

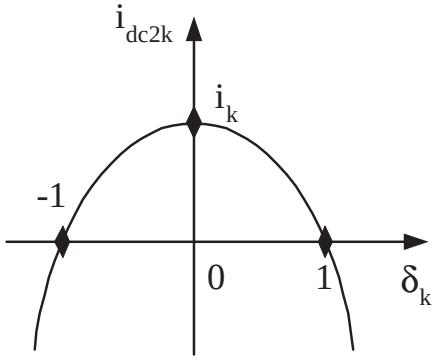

Figure 2.5: Description of the current functions i_{dc2k} using a quadratic function of δ_k, fitting all three points (♦), valid for each $k \in \{1, 2, 3\}$.

From $i_{dc2} = \sum_{k\in\{1,2,3\}} i_{dc2k}$, we obtain

$$\begin{aligned} i_{dc2} &= (1 - \delta_1^2)i_1 + (1 - \delta_2^2)i_2 + (1 - \delta_3^2)i_3 \\ &= -\delta_1^2 i_1 - \delta_2^2 i_2 - \delta_3^2 i_3 \end{aligned} \tag{2.10}$$

where we used the fact that $i_1 + i_2 + i_3 = 0$

Remark 2.2 Another expression for i_{dc2k} without involving square terms δ_i^2, $(i \in \{1, 2, 3\})$, but still valid in all three points, is obtained by using absolute values $|\delta_i|$ as follows

$$i_{dc2} = -|\delta_1|i_1 - |\delta_2|i_2 - |\delta_3|i_3 \tag{2.11}$$

where the squares have been replaced by absolute values. □

C. Current i_{dc3}

The case of i_{dc3} is very similar to i_{dc1}. The distribution of the three points (for each switch position) and the quadratic function fitting them are presented in Fig.2.6. In this case the expression of the quadratic function relating current i_{dc3k} and δ_k is

$$i_{dc3k} = (\delta_k - 1)\frac{\delta_k i_k}{2}$$

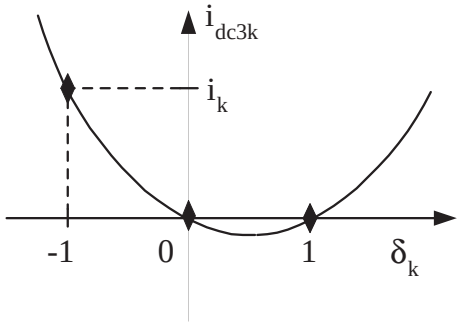

Figure 2.6: Description of the current functions i_{dc3k} using a quadratic function of δ_k, fitting all three points (♦), valid for each $k \in \{1, 2, 3\}$.

As before, from $i_{dc3} = \sum_{k\in\{1,2,3\}} i_{dc3k}$, it is obtained

$$i_{dc3} = (\delta_1 - 1)\frac{\delta_1 i_1}{2} + (\delta_2 - 1)\frac{\delta_2 i_2}{2} + (\delta_3 - 1)\frac{\delta_3 i_3}{2} \tag{2.12}$$

Direct substitution of (2.9), (2.10) and (2.12) in (2.7) and (2.8) yields the following expressions

$$\begin{aligned} C(\dot{v}_{C1} + \dot{v}_{C2}) &= i_{dc1} - i_{dc3} - 2i_R = \\ &= \delta_1 i_1 + \delta_2 i_2 + \delta_3 i_3 - \frac{2(v_{C1} + v_{C2})}{R} \end{aligned} \tag{2.13}$$

$$C(\dot{v}_{C1} - \dot{v}_{C2}) = i_{dc2} = -\delta_1^2 i_1 - \delta_2^2 i_2 - \delta_3^2 i_3 \tag{2.14}$$

Remark 2.3 It was observed in (2.13) that selecting as output the sum of the capacitors voltages automatically cancels the squares of δ_i, $(i \in \{1, 2, 3\})$ which appeared originally in the description of i_{dc1} and i_{dc3}. This, however, is not the case in the difference between the capacitors voltages as observed in (2.14) where the quadratic terms remain. □

Remark 2.4 Another option to describe the dynamics (2.14) without involving the square functions is considering the absolute value description of i_{dc2}, that is,

$$C\frac{d}{dt}(v_{C1}-v_{C2}) = -|\delta_1|i_1 - |\delta_2|i_2 - |\delta_3|i_3$$

Although this expression looks simpler than (2.14), it is more difficult to handle, specially while performing the transformation to $\alpha\beta$ coordinates, as it will become clear later. □

Summarizing, the overall model of system shown in Fig.2.2 is given by

$$\begin{bmatrix} L\frac{di_1}{dt} \\ L\frac{di_2}{dt} \\ L\frac{di_3}{dt} \end{bmatrix} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} v_{S1} \\ v_{S2} \\ v_{S3} \end{bmatrix} \tag{2.15}$$

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \frac{v_{C2}-v_{C1}}{2} \begin{bmatrix} \delta_1^2 \\ \delta_2^2 \\ \delta_3^2 \end{bmatrix} + \frac{v_{C2}+v_{C1}}{2} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} \tag{2.16}$$

$$C\frac{d}{dt}(v_{C1}+v_{C2}) = [\delta_1,\, \delta_2,\, \delta_3] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + \frac{2(v_{C1}+v_{C2})}{R} \tag{2.17}$$

$$C\frac{d}{dt}(v_{C1}-v_{C2}) = -[\delta_1^2,\, \delta_2^2,\, \delta_3^2] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{2.18}$$

which can also be expressed in matrix form as

$$L\frac{di_{123}}{dt} = -\frac{1}{3}Bv_{123} + v_{S123} \tag{2.19}$$

$$v_{123} = \frac{v_{C2}-v_{C1}}{2}[\delta_1^2,\, \delta_2^2,\, \delta_3^2]^\top + \frac{v_{C2}+v_{C1}}{2}\delta_{123} \tag{2.20}$$

$$C(\dot{v}_{C1}+\dot{v}_{C2}) = \delta_{123}^\top i_{123} - \frac{2(v_{C1}+v_{C2})}{R} \tag{2.21}$$

$$C(\dot{v}_{C1}-\dot{v}_{C2}) = -[\delta_1^2,\, \delta_2^2,\, \delta_3^2]i_{123} \tag{2.22}$$

where $i_{123} = [i_1,\, i_2,\, i_3]^\top$, $v_{S123} = [v_{S1},\, v_{S2},\, v_{S3}]^\top$, $v_{123} = [v_1,\, v_2,\, v_3]^\top$, $\delta_{123} = [\delta_1,\, \delta_2,\, \delta_3]^\top$ and

$$B = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

where it was noticed that the natural variables of interest are, besides the inductor currents, the sum and the difference of the capacitor voltages.

Remark 2.5 Under the consideration that $v_{C2} \cong v_{C1}$, subsystem (2.19) can be approximated as (2.6), which in matrix form can be written as

$$L\frac{di_{123}}{dt} = -\frac{v_{C1}+v_{C2}}{6}B\delta_{123} + v_{S123} \tag{2.23}$$

□

2.2.3 Transformation to $\alpha\beta\gamma$-coordinates

Vectors originally in abc-coordinates are transformed into $\alpha\beta\gamma$ coordinates according to

$$\begin{aligned} i_{\alpha\beta\gamma} &= Ti_{123} \quad , \quad v_{S\alpha\beta\gamma} = Tv_{S123} \\ \delta_{\alpha\beta\gamma} &= T\delta_{123} \quad , \quad v_{\alpha\beta\gamma} = Tv_{123} \end{aligned}$$

where $x_{\alpha\beta\gamma} \triangleq [x_\alpha,\, x_\beta,\, x_\gamma]^\top$ and the transformation matrix T used is defined as

$$T \triangleq \frac{2}{\sqrt{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

where $T^{-1} = \frac{1}{2}T^\top$, $TT^{-1} = \mathcal{I}_3$ and $\mathcal{I}_3$ is the 3×3 identity matrix.

Remark 2.6 The γ coordinate has been considered with the purpose to include an extra degree of freedom (DOF) present in the control vector. The γ coordinate will become crucial in the balance control of the capacitors voltages, as it will become clear later. □

Remark 2.7 For the control design purposes the *averaged model* is considered instead, i.e., the control inputs δ_1, δ_2 and δ_3 represent, from now on, continuous signals taking values in the range $[-1,\, 1]$. This is supported by the fact that, for the real implementation, an appropriate modulation technique, such as multi-carrier phase-shifted or level-shifted, with a relative high effective switching frequency is used. □

A. Inductor currents dynamics

Direct application of the above transformation on both sides of subsystem (2.19) gives

$$L\frac{dTi_{123}}{dt} = -TBT^{-1}v_{\alpha\beta\gamma} + Tv_{S123}$$

where $v_{123} = T^{-1}v_{\alpha\beta\gamma}$ has been used. This yields

$$L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta} + v_{S\alpha\beta} \tag{2.24}$$

where the fact that $TBT^{-1} = \text{diag}\{3, 3, 0\}$ has been used, $(i_1 + i_2 + i_3) = 0 \;\Rightarrow\; i_\gamma \equiv 0$ and $(v_{S1} + v_{S2} + v_{S3}) = 0 \;\Rightarrow\; v_{S\gamma} \equiv 0$.

From $v_{\alpha\beta\gamma} = T v_{123}$ the following expression for $v_{\alpha\beta}$ in terms of $\delta_{\gamma\alpha\beta}$ is obtained

$$v_{\alpha\beta} = \frac{2}{\sqrt{3}} \begin{bmatrix} v_1 - \frac{v_2+v_3}{2} \\ \frac{\sqrt{3}}{2}(v_2 - v_3) \end{bmatrix}$$

As described by (2.20)

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \frac{v_{C2} - v_{C1}}{2} \begin{bmatrix} \delta_1^2 \\ \delta_2^2 \\ \delta_3^2 \end{bmatrix} + \frac{v_{C2} + v_{C1}}{2} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix}$$

Vector $v_{\alpha\beta}$ can thus be computed as

$$v_{\alpha\beta} = \begin{bmatrix} \delta_1^2 - \frac{\delta_2^2+\delta_3^2}{2} & \frac{2}{\sqrt{3}}\left(\delta_1 - \frac{\delta_2+\delta_3}{2}\right) \\ \frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2) & \delta_2 - \delta_3 \end{bmatrix} \begin{bmatrix} \frac{v_{C2}-v_{C1}}{\sqrt{3}} \\ \frac{v_{C2}+v_{C1}}{2} \end{bmatrix} \tag{2.25}$$

On the other hand, using $\delta_{123} = T^{-1}\delta_{\alpha\beta\gamma}$ yields

$$\begin{aligned} \delta_1 &= \frac{1}{\sqrt{3}}\left(\frac{\delta_\gamma}{\sqrt{2}} + \delta_\alpha\right) \\ \delta_2 &= \frac{1}{\sqrt{3}}\left(\frac{\delta_\gamma}{\sqrt{2}} - \frac{\delta_\alpha}{2} + \frac{\sqrt{3}\delta_\beta}{2}\right) \\ \delta_3 &= \frac{1}{\sqrt{3}}\left(\frac{\delta_\gamma}{\sqrt{2}} - \frac{\delta_\alpha}{2} - \frac{\sqrt{3}\delta_\beta}{2}\right) \end{aligned} \tag{2.26}$$

On the right hand side of (2.25) the terms $\delta_1^2 - \frac{1}{2}(\delta_2^2 + \delta_3^2)$, $\frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2)$, $\frac{2}{\sqrt{3}}\left(\delta_1 - \frac{\delta_2+\delta_3}{2}\right)$ and $\delta_2 - \delta_3$ can be identified. They can be computed in terms of $\delta_{\gamma\alpha\beta}$ using (2.26) as follows

$$\delta_1^2 - \frac{1}{2}(\delta_2^2 + \delta_3^2) = \frac{\delta_\gamma\delta_\alpha}{\sqrt{2}} + \frac{\delta_\alpha^2 - \delta_\beta^2}{4} \tag{2.27}$$

$$\frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2) = \frac{\delta_\gamma\delta_\beta}{\sqrt{2}} - \frac{\delta_\alpha\delta_\beta}{2} \tag{2.28}$$

$$\frac{2}{\sqrt{3}}\left(\delta_1 - \frac{\delta_2 + \delta_3}{2}\right) = \delta_\alpha \tag{2.29}$$

$$\delta_2 - \delta_3 = \delta_\beta \tag{2.30}$$

Voltages vector $v_{\alpha\beta}$ can be rewritten as

$$v_{\alpha\beta} = \begin{bmatrix} \frac{\delta_\gamma\delta_\alpha}{\sqrt{2}} + \frac{\delta_\alpha^2-\delta_\beta^2}{4} & \delta_\alpha \\ \frac{\delta_\gamma\delta_\beta}{\sqrt{2}} - \frac{\delta_\alpha\delta_\beta}{2} & \delta_\beta \end{bmatrix} \begin{bmatrix} \frac{v_{C2}-v_{C1}}{\sqrt{3}} \\ \frac{v_{C2}+v_{C1}}{2} \end{bmatrix}$$

which can also be rewritten as

$$v_{\alpha\beta} = \frac{v_{C2} - v_{C1}}{\sqrt{3}} \begin{bmatrix} \frac{\delta_\gamma\delta_\alpha}{\sqrt{2}} + \frac{\delta_\alpha^2-\delta_\beta^2}{4} \\ \frac{\delta_\gamma\delta_\beta}{\sqrt{2}} - \frac{\delta_\alpha\delta_\beta}{2} \end{bmatrix} + \frac{v_{C2} + v_{C1}}{2}\delta_{\alpha\beta} \tag{2.31}$$

Remark 2.8 Notice, from (2.24) and (2.31), that the control component δ_γ has influence over the dynamics of $i_{\alpha\beta}$, however, this influence disappears as the voltages difference $(v_{C1} - v_{C2})$ approaches to zero. □

Remark 2.9 Following approximation (2.23), that is, considering $v_{C2} \cong v_{C1}$, the expression for subsystem (2.24), with $v_{\alpha\beta}$ described as in (2.31), can be reduced to

$$L\frac{di_{\alpha\beta}}{dt} = -\left(\frac{v_{C1} + v_{C2}}{2}\right)\delta_{\alpha\beta} + v_{S\alpha\beta} \tag{2.32}$$

which can be also obtained by applying the transformation directly to the approximation (2.23). □

B. Sum of the capacitors voltages

Applying the transformation to the sum of the capacitors voltages dynamics (2.21) yields

$$\begin{aligned} C(\dot{v}_{C1} + \dot{v}_{C2}) &= (T^{-1}\delta_{\alpha\beta\gamma})^\top T^{-1} i_{\alpha\beta\gamma} - \frac{2}{R}(v_{C1} + v_{C2}) \\ &= \frac{1}{2}\delta_{\alpha\beta\gamma}^\top i_{\alpha\beta\gamma} - \frac{2}{R}(v_{C1} + v_{C2}) \end{aligned}$$

but $i_\gamma = 0$, therefore

$$C(\dot{v}_{C1} + \dot{v}_{C2}) = \frac{1}{2}\delta_{\alpha\beta}^\top i_{\alpha\beta} - \frac{2}{R}(v_{C1} + v_{C2}) \tag{2.33}$$

Remark 2.10 Notice that the δ_γ component of the controller has not direct influence on the dynamics of the sum of the capacitors voltages. □

C. Difference of the capacitors voltages

Applying the transformation to the difference between the capacitor voltages dynamics (2.22) yields

$$C(\dot{v}_{C1} - \dot{v}_{C2}) = -[\delta_1^2,\, \delta_2^2,\, \delta_3^2]T^{-1} i_{\alpha\beta\gamma} \tag{2.34}$$

Compute of the first product yields

$$[\delta_1^2,\, \delta_2^2,\, \delta_3^2]T^{-1} =$$

$$\frac{1}{\sqrt{3}}\left[\delta_1^2 - \frac{1}{2}(\delta_2^2 + \delta_3^2),\, \frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2),\, \frac{1}{\sqrt{2}}(\delta_1^2 + \delta_2^2 + \delta_3^2)\right] \tag{2.35}$$

On the right hand side of this product the terms $\frac{1}{\sqrt{2}}(\delta_1^2 + \delta_2^2 + \delta_3^2)$, $\delta_1^2 - \frac{1}{2}(\delta_2^2 + \delta_3^2)$ and $\frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2)$ can be easily identified. The former is not necessary as $i_\gamma \equiv 0$, the remaining two were computed before in terms of $\delta_{\alpha\beta\gamma}$ in (2.27)-(2.28) giving

$$\begin{aligned} \delta_1^2 - \frac{1}{2}(\delta_2^2 + \delta_3^2) &= \frac{1}{\sqrt{2}}\delta_\gamma\delta_\alpha + \frac{1}{4}(\delta_\alpha^2 - \delta_\beta^2) \\ \frac{\sqrt{3}}{2}(\delta_2^2 - \delta_3^2) &= \frac{1}{\sqrt{2}}\delta_\gamma\delta_\beta - \frac{1}{2}\delta_\alpha\delta_\beta \end{aligned}$$

Remark 2.11 As pointed out before, the square functions can be replaced by absolute values, however, in this case the computations would be much more involved. □

Product (2.35) can now be written in terms of δ_α, δ_β and δ_γ as

$$[\delta_1^2,\ \delta_2^2,\ \delta_3^2]T^{-1} =$$

$$\frac{1}{\sqrt{3}}\left[\frac{1}{\sqrt{2}}\delta_\gamma\delta_\alpha + \frac{1}{4}(\delta_\alpha^2 - \delta_\beta^2),\ \frac{1}{\sqrt{2}}\delta_\gamma\delta_\beta - \frac{1}{2}\delta_\alpha\delta_\beta,\ *\right]$$

Direct substitution of the previous result in (2.34), with $i_\gamma = 0$, yields

$$\begin{aligned} C(\dot{v}_{C1} - \dot{v}_{C2}) &= -\left(\frac{\delta_{\alpha\beta}^\top i_{\alpha\beta}}{\sqrt{6}}\right)\delta_\gamma \\ &\quad -\frac{1}{4\sqrt{3}}\left[\delta_\alpha^2 - \delta_\beta^2,\ -2\delta_\alpha\delta_\beta\right] i_{\alpha\beta} \end{aligned} \tag{2.36}$$

Remark 2.12 From (3.3) it can be observed that the control component δ_γ has a direct influence over the dynamics of the difference of capacitors voltages. However, this control component is affected by the projection $\delta_{\alpha\beta}^\top i_{\alpha\beta}$, therefore special attention should be taken in the control design process to keep such a projection bounded away from zero. □

Summarizing, the model of the three level converter in $\alpha\beta\gamma$-coordinates is given by

$$L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta} + v_{S\alpha\beta} \tag{2.37}$$

$$\begin{aligned} v_{\alpha\beta} &= \frac{v_{C2} - v_{C1}}{\sqrt{3}}\begin{bmatrix} \frac{\delta_\gamma\delta_\alpha}{\sqrt{2}} + \frac{\delta_\alpha^2 - \delta_\beta^2}{4} \\ \frac{\delta_\gamma\delta_\beta}{\sqrt{2}} - \frac{\delta_\alpha\delta_\beta}{2} \end{bmatrix} \\ &\quad + \frac{v_{C2} + v_{C1}}{2}\delta_{\alpha\beta} \end{aligned} \tag{2.38}$$

$$C(\dot{v}_{C1} + \dot{v}_{C2}) = \frac{1}{2}\delta_{\alpha\beta}^\top i_{\alpha\beta} - \frac{2}{R}(v_{C1} + v_{C2}) \tag{2.39}$$

$$\begin{aligned} C(\dot{v}_{C1} - \dot{v}_{C2}) &= -\frac{1}{4\sqrt{3}}\left[\delta_\alpha^2 - \delta_\beta^2,\ -2\delta_\alpha\delta_\beta\right] i_{\alpha\beta} \\ &\quad -\left(\frac{\delta_{\alpha\beta}^\top i_{\alpha\beta}}{\sqrt{6}}\right)\delta_\gamma \end{aligned} \tag{2.40}$$

2.3 Model verification

A three level converter and the proposed model have been simulated and compared to show the validity of the proposed one. The former includes the effects of the switching devices and is controlled by a switching sequence, while the latter is controlled by the average continuous control signals $\delta_{\alpha\beta\gamma}$ obtained from a conventional control. The pulses for the switching system are generated using a modulation algorithm referred as SVM-3D that was proposed in [24], having as inputs the same control signals $\delta_{\alpha\beta\gamma}$. This generalized method easily provides the nearest switching vectors sequence to the reference vector and calculates

the on-state durations of the respective switching state vectors without involving trigonometric functions, look-up tables or coordinate system transformations which increase the computational load corresponding to the modulation of multilevel converters. The following conditions have been considered in the simulations: sampling frequency 10KHz, capacitance $C = 3300\,\mu$F, inductance $L = 1.2$mH, reference for the sum of voltages 700V. The test consists in changing the load from $R = 20\,\Omega$ to $R = 10\,\Omega$ at $t = 0.2$s. Every figure shows the response using the proposed model in the top plot and the response of the switching system driven by pulses in the bottom plot. Figure 2.7 shows the time responses of the input currents $i_{\alpha\beta}$ to the load change. Figure 2.8 shows the time responses of the sum of voltages $x_3 = v_{C1} + v_{C2}$. And Fig.2.9 shows the responses of the voltages difference $x_3 = v_{C1} - v_{C2}$.

Experimental results are shown in the chapter 3 in order to validate the proposed model and to show the benefits of the proposed controller.

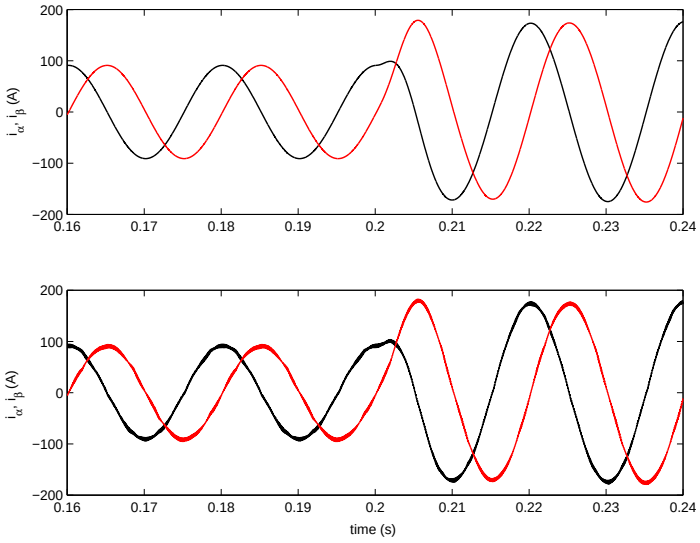

Figure 2.7: Input currents $i_{\alpha\beta}$ responses to a load step change from 20Ω to 10Ω at $t = 0.2$s: **(Top)** Proposed model and **(Bottom)** switching system driven by pulses.

2.4 Conclusions

In this chapter is presented a model for the three-level NPC converter. The model was obtained in the original abc-coordinates and then after transformations it was also presented in $\alpha\beta\gamma$-coordinates. It was found that a natural way to write the model is considering as variables the sum and the difference of the capacitors voltages, besides the inductors currents. The proposed model stressed the existence of a third degree of freedom (DOF) offered by the control input, and referred here as the γ-component, which, together with the α and β components, form the control input vector.

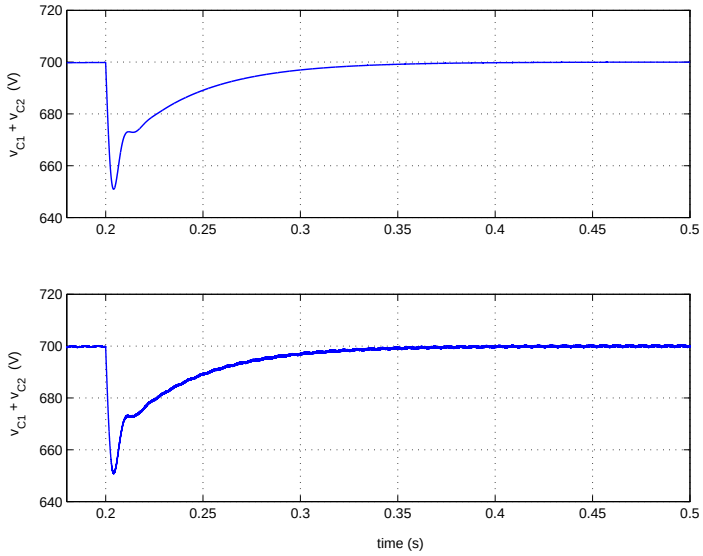

Figure 2.8: Sum of voltages $x_3 = v_{C1} + v_{C2}$ responses to a load step change from 20Ω to 10Ω at $t = 0.2$s: **(Top)** Proposed model and **(Bottom)** switching system driven by pulses

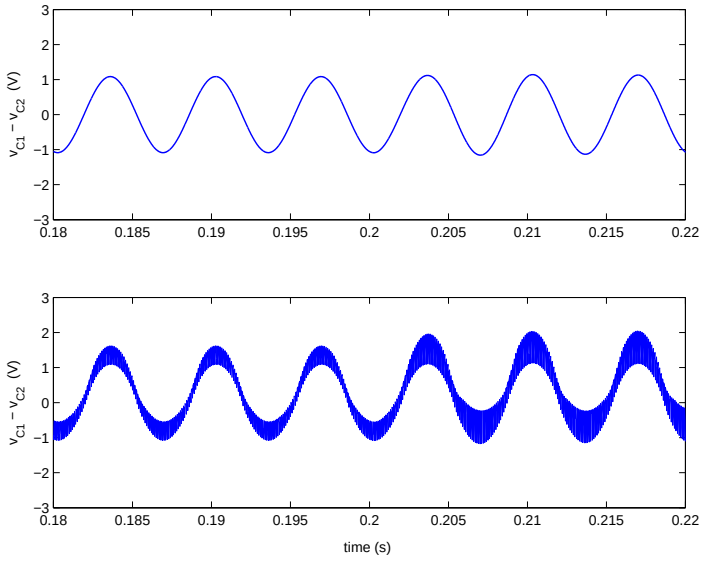

Figure 2.9: Difference of voltages $x_4 = v_{C1} - v_{C2}$ responses to a load step change from 20Ω to 10Ω at $t = 0.2$s: **(Top)** Proposed model and **(Bottom)** switching system driven by pulses

Chapter 3

NPC Multilevel Converter: Adaptive Controller for a Three-level Synchronous Rectifier

3.1 Introduction

Based on the model described in the previous chapter, the capacitors voltage balancing issue can now be treated from another viewpoint. The main feature of the previously proposed model is the existence of a third degree of freedom (DOF) offered by the control input referred as the γ component, which is put in evidence, and together with the α and β components form the control input vector. It is shown that this γ component is precisely the DOF required to pursue the capacitors voltages balance. The model is written in terms of the sum and the difference of the capacitors voltages, which are perhaps the natural variables, besides the inductors currents. According to this description, to guarantee the capacitors voltages balance, is equivalent to drive to zero the difference of capacitors voltages. It is observed that the dynamics associated to this voltages difference is being perturbed by higher order harmonics, mainly a third harmonic. Therefore, the proposed controller includes an adaptive term to cope with these disturbances. After some transformations, this adaptive term is finally reduced to a bank of resonant filters. The proposed controller thus guarantees regulation, balance of the capacitors voltages, and a close to unity power factor. Numerical results are presented to asses the performance of the proposed controller.

3.2 Model of the three level inverter

The basic setup for the synchronous rectifier application using a three level NPC inverter discussed in this chapter is shown in Fig.2.1, and the equivalent circuit with ideal switches is shown in Fig.2.2 in the previous chapter.

The system dynamics is described by the following model in $\alpha\beta\gamma$-coordinates (the γ coordinate is also referred as coordinate "0" in the literature), which was obtained in the

previous chapter.

$$L\frac{di_{\alpha\beta}}{dt} = -\frac{v_{C1}+v_{C2}}{2}\delta_{\alpha\beta} + v_{S\alpha\beta} \tag{3.1}$$

$$C(\dot{v}_{C1}+\dot{v}_{C2}) = \frac{1}{2}\delta_{\alpha\beta}^{\top} i_{\alpha\beta} - \frac{2}{R}(v_{C1}+v_{C2}) \tag{3.2}$$

$$C(\dot{v}_{C1}-\dot{v}_{C2}) = -\frac{1}{4\sqrt{3}}\left[\delta_{\alpha}^{2}-\delta_{\beta}^{2},\ -2\delta_{\alpha}\delta_{\beta}\right] i_{\alpha\beta} - \left(\frac{\delta_{\alpha\beta}^{\top} i_{\alpha\beta}}{\sqrt{6}}\right)\delta_{\gamma} \tag{3.3}$$

where

$v_{S\alpha},\ v_{S\beta}$	:	source voltages
$i_{\alpha},\ i_{\beta}$	:	inductor currents
$v_{C1},\ v_{C2}$	:	capacitors voltages
$\delta_{\alpha},\ \delta_{\beta},\ \delta_{\gamma}$	:	control signals $\in \{-1, 0, 1\}$
L	:	inductance of input inductors
C	:	capacitance of output capacitors
R	:	load resistance

Remark 3.1 From (3.3) it was observed that the control component δ_{γ}, usually disregarded in most three-phase three-wire applications, has a direct influence over the dynamics of the difference of capacitors voltages, and thus it will be crucial in the balancing of the capacitors voltages. However, this control component, as observed in (3.3) is affected by the projection $\delta_{\alpha\beta}^{\top} i_{\alpha\beta}$. Therefore, special attention should be taken in the control design process to keep such a projection bounded away from zero. □

3.3 Controller design

To simplify the notation, the following transformations are considered

$$x_1 = i_{\alpha},\ \ x_2 = i_{\beta},\ \ x_3 = v_{C1}+v_{C2},\ \ x_4 = v_{C1}-v_{C2}$$

$$u_1 = \delta_{\alpha},\ \ u_2 = \delta_{\beta},\ \ u_3 = \delta_{\gamma},\ \ v_S = v_{S\alpha\beta}$$

The model can then be rewritten as

$$L\dot{x}_{12} = -\frac{1}{2}x_3 u_{12} + v_S \tag{3.4}$$

$$C\dot{x}_3 = \frac{1}{2}u_{12}^{\top} x_{12} - \frac{2}{R}x_3 \tag{3.5}$$

$$C\dot{x}_4 = -\frac{1}{4\sqrt{3}}\left[(u_1^2-u_2^2),\ -2u_1u_2\right] x_{12} - \frac{1}{\sqrt{6}}u_3 u_{12}^{\top} x_{12} \tag{3.6}$$

The multilevel converter presented here is used in an application of a three-phase rectifier. The *control objective* can be stated, in terms of the new variables, as follows:

i) First, a power factor close to the unity should be guaranteed. This can be fulfilled if

$$x_{12} \rightarrow x_{12}^* = g v_S \ , \ \ x_{12} = [x_1 \ , \ x_2]^\top$$

that is, the input current signal follows a signal proportional to the supplied voltage. The proportionality gain g represents the equivalent conductance observed by the power supply, and represents a degree of freedom yet to be defined.

ii) Second, the controller should regulate the sum of the output capacitors voltages towards a desired constant reference V_d, that is,

$$x_3 \rightarrow x_3^* = V_d$$

iii) Third, the voltage in both capacitors should be balanced. In other words, the difference between the capacitors voltages should be driven to zero, that is,

$$x_4 \rightarrow x_4^* = 0$$

Here and in what follows $(\cdot)^*$ is used to represent a desired reference. Also, the simplified notation $x_{12} = [x_1, \ x_2]^\top$ and $u_{12} = [u_1 \ , \ u_2]^\top$ is used to represent vectors.

3.3.1 Main assumptions

A1. It is of great interest to design robust controllers with respect to parameter uncertainties, and thus, in the control design process, most system parameters are considered as unknown constants, possibly changing in steps, or that can be slowly varying.

A2. To facilitate the control design, it is assumed that x_{12} dynamics is much faster than the dynamics of x_3 and x_4, and thus, these two latter can be decoupled from the former based on a time scale separation argument.

A3. It is assumed that $i_\gamma = 0, \ v_{S\gamma} = 0$ because there is not connection to neutral, that is, no homopolar component is considered, and also equilibrated voltages can be assumed.

A4. In this first approach it is considered that the source voltage is composed mainly by its fundamental component, that is, it can be expressed as

$$v_S(t) = e^{Jwt} V_S \ \ , \ \ \ e^{Jwt} = \begin{bmatrix} \cos(wt) & -\sin(wt) \\ \sin(wt) & \cos(wt) \end{bmatrix}$$

$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$$

where $V_S = [V_S^r, \ V_S^i]$ represents the phasor vector of signal $v_S(t)$, with V_S^r and V_S^i the real and imaginary parts, respectively, both considered as unknown constants and J is a skew symmetric matrix. Notice that, in this special case, the current reference can be represented as

$$x_{12}^* = g e^{Jwt} V_S$$

whose time derivative, extremely useful in solving the tracking problem, is given by

$$\dot{x}_{12}^* = gwJv_S = wJx_{12}^*$$

where it has been considered $\dot{g} \cong 0$, based on the decoupling assumption.

The control design process is thus divided in three steps. First, a controller for x_{12} is proposed to solve the current tracking problem. This controller is referred as *inner or current control loop*. Second, a controller that regulates x_3 towards its constant reference is designed. This controller is addressed as the *outer or voltage control loop*. Finally, a controller that zeroes x_4 is proposed. This last controller is referred as the *voltage balancing control*.

3.3.2 Inner (current) control loop

Consider subsystem (3.4) describing the inductor currents x_{12} dynamics

$$L\dot{x}_{12} = -\nu_{12}$$

where $\nu_{12} \stackrel{\triangle}{=} \frac{1}{2}x_3 u_{12} - v_S$ has been defined.

Notice that, in the case that all parameters are known, the following controller solves the tracking problem

$$\nu_{12} = -L\dot{x}_{12}^* + k_1\tilde{x}_{12} = -LwJx_{12}^* + k_1\tilde{x}_{12} = -\theta Jx_{12}^* + k_1\tilde{x}_{12}$$

where k_1 is a positive design parameter, $\tilde{x}_{12} \stackrel{\triangle}{=} x_{12} - x_{12}^*$ and $\theta \stackrel{\triangle}{=} wL$.

Since in the previous controller both parameters L and possibly w are unknown constants, it is proposed the following controller instead

$$\nu_{12} = -\hat{\theta}Jx_{12}^* + k_1\tilde{x}_{12}$$

where $\hat{\theta}$ represents the estimate of the unknown θ.

The error dynamics is given by

$$L\dot{\tilde{x}}_{12} = -k_1\tilde{x}_{12} + \tilde{\theta}Jx_{12}^* \tag{3.7}$$

where $\tilde{\theta} \stackrel{\triangle}{=} \hat{\theta} - \theta$.

The adaptive law is designed by following the Lyapunov approach, for this, the following quadratic function is proposed

$$H = \frac{L}{2}\tilde{x}_{12}^\top\tilde{x}_{12} + \frac{1}{2\gamma}\tilde{\theta}^2$$

whose time derivative along the trajectories of (3.7) is

$$\dot{H} = -k_1\tilde{x}_{12}^\top\tilde{x}_{12} + \tilde{\theta}\tilde{x}_{12}^\top Jx_{12}^* + \frac{1}{\gamma}\tilde{\theta}\dot{\tilde{\theta}}$$

Out of which the following adaptive law is proposed

$$\dot{\hat{\theta}} = -\gamma\tilde{x}_{12}^\top Jx_{12}^*$$

where γ is a positive design parameter, referred as the adaptation gain. Notice that, the fact $\dot{\tilde{\theta}} = \dot{\hat{\theta}}$ has been used, since θ is assumed constant. This yields

$$\dot{H} = -k_1\tilde{x}_{12}^\top\tilde{x}_{12}$$

The proof follows using Barbalat's lemma [45]. From the proposed adaptive law, all error signals are bounded, i.e. $\tilde{x}_{12}$ in L_∞, $\tilde{\theta}$ in L_∞, equivalently the estimate state is bounded as well, i.e. $\hat{\theta}$ in L_∞. This implies that the time derivate of the error is bounded as well, i.e. $\dot{\tilde{x}_{12}}$ in L_∞. From the Barbalat's lemma then $\dot{H} \rightarrow 0$ as $t \rightarrow \infty$ and hence $\tilde{x}_{12} \rightarrow 0$, which is asymptotically stable.

Summarizing, the proposed inner (current) controller is given by

$$\boxed{\begin{array}{rcl} u_{12} & = & \dfrac{2}{x_3}\left(v_S - \hat{\theta} J x_{12}^* + k_1 \tilde{x}_{12}\right) \\ \dot{\hat{\theta}} & = & -\gamma \tilde{x}_{12}^\top J x_{12}^* \\ \tilde{x}_{12} & = & x_{12} - x_{12}^* \ , \quad x_{12}^* = g v_S \end{array}} \tag{3.8}$$

3.3.3 Outer (voltage) control loop

Based on the decoupling assumption, after a relatively short time, $\tilde{x}_{12} \cong 0$, $\tilde{\theta} \cong 0$ and $u_{12} = u_{12eq}$ where

$$u_{12eq} = u_{12}|_{\{\tilde{x}_{12}=0,\, \tilde{\theta}=0\}} = \frac{2}{x_3}\left(vs - gwLJv_S\right)$$

is the equivalent controller.

From (5.23), the dynamics of the sum of voltages x_3 gets the form

$$C\dot{x}_3 = \frac{1}{2} u_{eq12}^\top x_{12}^* - \frac{2}{R} x_3$$

Direct substitution of u_{eq12} in the expression above yields

$$Cx_3\dot{x}_3 = (vs - gwLJv_S)^\top g v_S - \frac{2}{R}x_3^2 = v_S^\top v_S g - \frac{2}{R}x_3^2$$

Considering the transformation $z_3 = x_3^2/2$, the system above can be rewritten as

$$C\dot{z}_3 = g v_S^\top v_S - \frac{4}{R} z_3 \tag{3.9}$$

which is a stable first order system having as control input the variable g which is affected by a positive bounded function $v_S^\top v_S$.

According to the first control objective, x_3 should be regulated to a desired constant reference. However, since x_3 and thus z_3 have an unavoidable ripple, this control objective can be only accomplished in average, for this purpose, the dc component of (5.14) is considered only as follows

$$C\dot{z}_{30} = \langle g v_S^\top v_S \rangle_0 - \frac{4}{R} z_{30}$$

where $\langle \cdot \rangle_0$ is a function that extracts the dc component of a signal, and $z_{30} = \langle z_3 \rangle_0$. The extraction of the the dc component of a scalar x is defined, at time t, by the following averaging operation $\langle x \rangle_0(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau) d\tau$, referred also as the moving average.

Recalling that the control signal g affects the current reference in the form $x_{12}^* = gv_S$, it should then be proposed a controller that forces g to converge as smooth as possible towards a constant in the steady state. Towards this end, it is assumed that $\langle gv_S^\top v_S\rangle_0 \cong g\langle v_S^\top v_S\rangle_0 = gv_{S,RMS}^2$ where $v_{S,RMS}$ is the RMS value of v_S. Moreover, as it is common practice, the control input is redefined as $G \triangleq gv_{S,RMS}^2$, this yields

$$C\dot{z}_{30} = G - \frac{4}{R}z_{30} \tag{3.10}$$

For this first order system, the following controller is proposed

$$\begin{aligned} G &= -k_p\chi - k_i\xi && (3.11)\\ \tau\dot{\chi} &= -\chi + \tilde{z}_{30} && (3.12)\\ \dot{\xi} &= \tilde{z}_{30} && (3.13) \end{aligned}$$

where k_p and k_i are positive design constants, which are tuned in a similar way as in a PI controller, τ is also a positive design constant, and represents the time constant of a LPF. Parameter τ is selected small enough such that the LPF bandwidth is inferior to the 2nd order harmonic of the fundamental. Indeed, following the classical Hurwitz criterium, it is possible to show that the closed loop system (3.10) and (3.11)-(3.13) is exponentially stable provided all design parameters are positive. Evidently, there are certain restrictions for the parameter values, which is linked to the decoupling assumption, basically, the response of this subsystem cannot be made arbitrarily fast.

Moreover, thanks to the low pass filtering properties of the LPF (3.12) and integrator (3.13), similar results can be obtained by using either z_3 or z_{30} in the controller implementation. Since z_{30} is not available, it is preferred to use z_3 in the implementation. Summarizing, the expressions conforming the outer loop controller are given by

$$\boxed{\begin{aligned} G &= -k_p\chi - k_i\xi\\ \tau\dot{\chi} &= -\chi + \tilde{z}_3\\ \dot{\xi} &= \tilde{z}_3 \end{aligned}} \tag{3.14}$$

3.3.4 Voltage balancing control

In this section, a controller is presented to balance the voltage in the capacitors, in other words, to bring to zero the difference between the capacitors voltages $x_4 = v_{C1} - v_{C2}$. For easy of reference, the differential equation describing these dynamics are rewritten next

$$C\dot{x}_4 = -\frac{1}{\sqrt{6}}(u_{12}^\top x_{12})u_3 - \frac{1}{4\sqrt{3}}\left[u_1^2 - u_2^2,\ \ -2u_1u_2\right]x_{12} \tag{3.15}$$

If the interest was to control the average value of x_4 only, then this problem falls into a classical regulation problem. However, as it will become clear later, there is an important contribution of harmonics due to the second term on the RHS of (3.15). The proposed controller should then guarantee both, regulation and harmonic disturbances rejection.

As in the previous section, based on the decoupling assumption, it is considered that after a relatively short time the following holds

$$x_{12} = x_{12}^* = g v_S \ , \quad u_{12} = u_{12eq} \tag{3.16}$$

where

$$\begin{aligned} u_{12eq} &= u_{12}|_{\{\tilde{x}_{12}=0,\,\tilde{\theta}=0\}} = \frac{2}{x_3}(v_S - L\dot{x}_{12}^*) \\ &= \frac{2}{x_3}(I_2 - gwLJ)v_S \\ &= \frac{2}{x_3}\begin{bmatrix} v_{S1} + gwLv_{S2} \\ v_{S2} - gwLv_{S1} \end{bmatrix} \end{aligned} \tag{3.17}$$

with I_2 the 2×2 identity matrix, and J the skew symmetric matrix defined previously.

The system dynamics can now be written as

$$\begin{aligned} C\dot{x}_4 &= -\frac{1}{4\sqrt{3}}\left[(u_{1eq}^2 - u_{2eq}^2)x_1^* - 2u_{1eq}u_{2eq}x_2^*\right] \\ &\quad -\frac{1}{\sqrt{6}}(u_{12eq}^\top x_{12}^*)u_3 \end{aligned} \tag{3.18}$$

Direct substitution of (3.16)-(3.17) in (3.18) yields, term by term,

$$u_{12eq}^\top x_{12}^* = \frac{2}{x_3}\left[(I_2 - gwLJ)v_S\right]^\top g v_S = \frac{2}{x_3} g v_S^\top v_S$$

$$\begin{aligned} (u_{1eq}^2 - u_{2eq}^2)x_1^* &= \frac{4}{x_3^2}\left[(v_{S1}^2 - v_{S2}^2)(1 - g^2w^2L^2)\right. \\ &\quad \left. +4v_{S1}v_{S2}gwL\right] g v_{S1} \end{aligned}$$

$$\begin{aligned} -2u_{1eq}u_{2eq}x_2^* &= \frac{4}{x_3^2}\left[2gwL(v_{S1}^2 - v_{S2}^2)\right. \\ &\quad \left. -2v_{S1}v_{S2}(1 - g^2w^2L^2)\right] g v_{S2} \end{aligned}$$

Out of which the difference of capacitors voltages dynamics become

$$C\dot{x}_4 = -\left(\sqrt{\frac{2}{3}}\frac{g}{x_3} v_S^\top v_S\right) u_3 - \frac{g}{\sqrt{3}x_3^2}\delta(t) \tag{3.19}$$

where all distorting terms have been concentrated in a single variable $\delta(t)$, that is,

$$\begin{aligned} \delta(t) &= (1 - g^2w^2L^2)v_{S1}^3 + 6gwLv_{S1}^2v_{S2} \\ &\quad -3(1 - g^2w^2L^2)v_{S2}^2v_{S1} - 2gwLv_{S2}^3 \end{aligned}$$

Remark 3.2 Notice that, $\delta(t)$ is composed by products of the form v_{S1}^3, $v_{S1}^2v_{S2}$, $v_{S2}^2v_{S1}$ and v_{S2}^3. Therefore, it is expected that the harmonic content of $\delta(t)$ will be composed mainly by fundamental and third harmonic. Recall for instance that, $\cos^3(wt) = \frac{1}{4}(\cos(3wt) + 3\cos(wt))$, $\sin^2(wt)\cos(wt) = -\frac{1}{4}(\cos(3wt) - \cos(wt))$, etc. □

For the sake of clarity in the control design process, it is convenient to define

$$\begin{aligned} \phi(t) &\triangleq \frac{g}{\sqrt{3}x_3^2}\delta(t) \\ \nu_3 &\triangleq \left(\sqrt{\frac{2}{3}}\frac{g}{x_3}v_S^\top v_S\right)u_3 \end{aligned}$$

The system (3.19) is thus reduced to

$$C\dot{x}_4 = -\nu_3 - \phi \tag{3.20}$$

Remark 3.3 Notice that, if g and x_3 are smooth enough, as demanded in normal operation, then the harmonics content of $\phi(t)$ is similar to that of $\delta(t)$. □

It is assumed that signal ϕ can be described as the sum of its harmonic components (mainly first and third harmonic components as stated before) as follows

$$\phi = \sum_{k\in\{1,3\}} \rho_k^\top \Phi_k \quad , \quad \rho_k = \begin{bmatrix} \cos(kwt) \\ \sin(kwt) \end{bmatrix} \quad , \quad \Phi_k = \begin{bmatrix} \Phi_k^r \\ \Phi_k^i \end{bmatrix}$$

where $\Phi_k \in \mathbb{R}^2$ is the phasor, assumed to be an unknown constant vector, of the kth harmonic component of ϕ.

The following controller is proposed

$$\begin{aligned} \nu_3 &= k_b\chi + \hat{\phi} \\ \sigma\chi &= -\chi + x_4 \end{aligned}$$

where $\hat{\phi}$ represents the estimate of ϕ; k_b and σ are positive design constants.

Remark 3.4 Notice that there is not need of an integral action since no DC offset appears in system (3.20). □

Based on the previous description of ϕ it is assumed that

$$\hat{\phi} = \sum_{k\in\{1,3\}} \rho_k^\top \hat{\Phi}_k$$

where $\hat{\Phi}_k$ represents now the estimate for Φ_k.

The error system can then be rewritten as

$$C\dot{x}_4 = -k_b\chi + \sum_{k\in\{1,3\}} \rho_k^\top \tilde{\Phi}_k \tag{3.21}$$

$$\sigma\dot{\chi} = -\chi + x_4 \tag{3.22}$$

where $\tilde{\Phi}_k \triangleq \hat{\Phi}_k - \Phi_k$, $(k \in \{1,3\})$.

Following the Lyapunov approach to design adaptive laws to estimate $\hat{\Phi}_k$. Towards this end, it is proposed the following quadratic storage function

$$H = \frac{C}{2}x_4^2 + \frac{k_b\sigma}{2}\chi^2 + \sum_{k\in\{1,3\}} \frac{1}{2\gamma_k}\tilde{\Phi}_k^\top \tilde{\Phi}_k$$

whose time derivative along the trajectories of (3.21)-(3.22) yields

$$\dot{H} = -k_b\chi^2 + x_4 \sum_{k=1,3} \rho_k^\top \tilde{\Phi}_k + \sum_{k\in\{1,3\}} \frac{1}{\gamma_k}\dot{\tilde{\Phi}}_k^\top \tilde{\Phi}_k$$

Out of which the following adaptive laws are proposed

$$\dot{\hat{\Phi}}_k = -\gamma_k \rho_k x_4 \quad , \quad k \in \{1,3\}$$

where it has been used the fact that $\dot{\hat{\Phi}}_k = \dot{\tilde{\Phi}}_k$.

The adaptation scheme proposed above can be further simplified by considering the following transformations

$$\begin{aligned} \hat{\phi}_k &= \rho_k^\top \hat{\Phi}_k \quad , \quad k \in \{1,3\} \\ \hat{\psi}_k &= \rho_k^\top J \hat{\Phi}_k \end{aligned}$$

The adaptations are thus transformed in the following expressions

$$\begin{aligned} \dot{\hat{\phi}}_k &= -\gamma_k x_4 - kw\hat{\phi}_k \quad , \quad k \in \{1,3\} \\ \dot{\hat{\psi}}_k &= kw\hat{\phi}_k \end{aligned}$$

Notice that these expressions define indeed an LTI system which can be expressed in the form of a transfer function having as output the states $\hat{\phi}$ ($k \in 1,3$). This yields the following bank of resonant filters

$$\hat{\phi}_k = \frac{-\gamma_k s}{s^2 + k^2 w^2} x_4 \quad , \quad k \in \{1,3\}$$

Summarizing, the part of the controller that balance the capacitors voltages, i.e., that brings to zero the difference between the capacitors voltages, is given by

$$\boxed{\begin{aligned} u_3 &= \left(\sqrt{\frac{3}{2}}\frac{x_3}{g v_S^\top v_S}\right)\nu_3 \\ \nu_3 &= k_p\chi + \sum_{k\in\{1,3\}} \hat{\phi}_k \\ \sigma\chi &= -\chi + x_4 \\ \hat{\phi}_k &= \frac{-\gamma_k s}{s^2 + k^2 w^2} x_4 \quad , \quad k \in \{1,3\} \end{aligned}} \tag{3.23}$$

Remark 3.5 It has been assumed, so far, that the line frequency w is well known (and constant), this restriction, can be avoided by using an adaptive estimator that includes the estimation of w as well. However, in practice, this frequency does not vary considerably from

the nominal value. In fact, a slight mismatch does not have a serious effect on the response of the controller because the resonant filters are implemented by means of band pass filters with a limited quality factor. □

Remark 3.6 The term $gv_S^\top v_S$ is a scale factor multiplying the apparent conductance of the line g. This term could be substituted by $gv_{S,RMS}^2$, where $v_{S,RMS}$ is the RMS value of the source voltages vector, which could be considered a constant. □

Figure 3.1 depicts a detailed block diagram of the completed proposed controller.

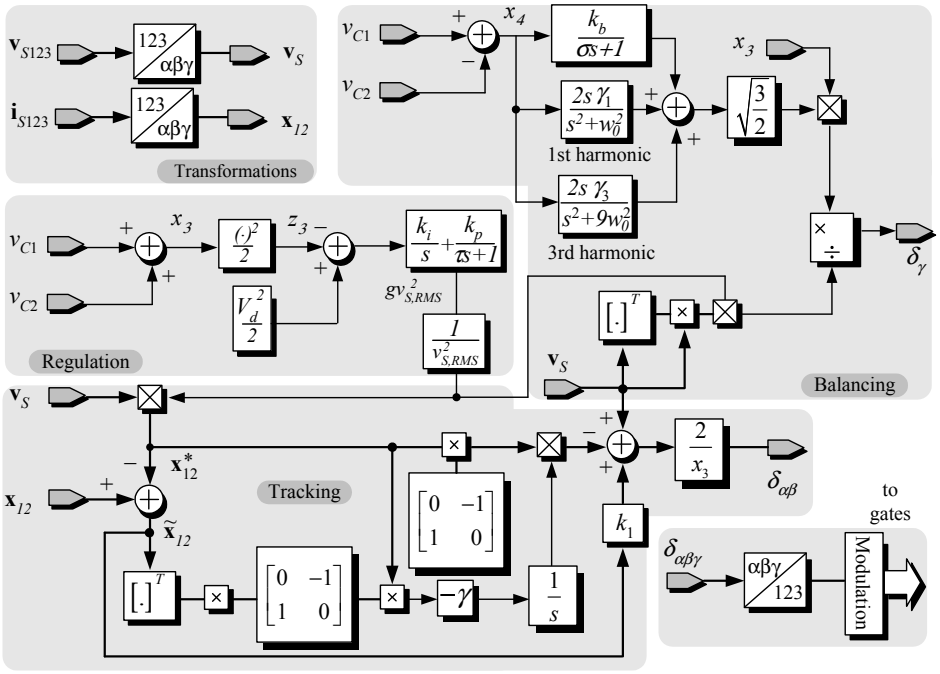

Figure 3.1: Block diagram of the overall controller including tracking, regulation and balance control loops.

3.4 Simulation results

The system (3.4)-(3.6) has been simulated together with the overall controller composed by the *inner control loop* (3.8), the *outer control loop* (3.14) and the *voltage balancing controller* (3.23). The reference for the sum of the capacitors voltages is set to $x_4^* = 700$ V (350 V on each capacitor). The load resistor is varied from 20 Ω to 10 Ω at $t = 0.66$ s, and back to 20 Ω at $t = 1.33$ s. The system parameters are $w = 100\pi$ rad/sec ($f = 50$ Hz), L =1.2 mH, C =6600 μF, $R \in \{10\,\Omega,\ 20\,\Omega\}$, $v_{S,RMS}$ =220 V_{RMS}.

The parameters of the controller are set to:

- ▷ Inner loop: $k_1 = 2.5$, $\gamma = 0.01$
- ▷ Outer loop: $k_p = 0.1$, $k_i = 3.75$, $\tau = 0.001$

▷ Balancing loop: $k_b = 0.75$, $\sigma = 0.001$, $\gamma_1 = 0$, $\gamma_3 = 10$

The bandwidth of the controller frequency response is limited by the maximum frequency of sampling/commutation. Usually, the bandwidth of the current loop is desired to be 1/10 of the sampling frequency. Based on this, an approximate procedure is followed to find an initial setting of the parameters for the current tracking control loop. First, it is proposed to set k_1 equal to $2\pi f_{ic}L$, where f_{ic} is the desired current loop bandwidth, in this case, $f_{ic} = f_{sw}/10$. Second, the remaining transfer function is a first order low pass filter having a pole at $2\pi f_{ic}$. Disregarding, for simplicity, the influence of such a pole, the gain γ can be set as $\gamma = T_{k\gamma}$, where $T_{k\gamma}$ is the desired response time evaluated between the 10% and 90% of a step response of the amplitude of the corresponding sinusoidal perturbation. This relation is exact only when different band-pass filters give independent contributions. In a general case, however, this procedure gives a useful estimate of controller parameters given the desired response time for various harmonic components.

In the first outer loop, corresponding to the regulation of the capacitor voltages, the parameter selection is guided by conventional techniques given the desired regulation loop bandwidth and phase margin. Note, however, that due to the ripple on the DC voltage at twice the supply frequency during unbalanced conditions, the voltage loop bandwidth should be limited to approximately 10-20 Hz in order to avoid possible amplification of the second harmonic in the line current reference.

In the second outer loop, corresponding to the balance of the capacitor voltages, the parameter selection is guided also by conventional techniques. The main consideration in this outer loop is that the response in frequency of the controllers is limited by the response in frequency of the first outer loop. The response in frequency in this loop is usually set 1/5 of the response in frequency of the regulation loop.

Figure 3.2 shows the transient response of both input currents to a load step change from $20\,\Omega$ to $10\,\Omega$ at $t = 0.66$ s. In the same plots, are included the corresponding source voltages in dotted lines to exhibit the fulfilment of and almost unitary power factor.

Figure 3.3 shows the transient response of capacitors voltages sum $x_3 = v_{C1} + v_{C2}$ and difference $x_4 = v_{C1} - v_{C2}$ during a load resistor change from 20 Ω to 10 Ω at $t = 0.66$ s, and back to 20 Ω at $t = 1.33$ s. It is observed that after relatively small transients the sum x_3 converges towards its desired constant reference $V_d = 700$ V, while the difference of capacitors voltages x_4 converges almost to zero, thanks to the harmonics cancelation. Figure 3.4 compares the responses of the difference of capacitors voltages x_4 obtained with the harmonics compensation strategy (in the bottom plot), and without harmonic compensation (in the top plot). Notice that, without harmonic compensation there is a non vanishing ripple, actually a third harmonic, of almost constant amplitude.

Finally, Fig. 3.5 shows the plots of the gain $g = G/v_{S,RMS}^2$ and the estimated parameter $\hat{\theta} = \widehat{wL}$. Notice that, while $\hat{\theta}$ converges to the real value $\theta = wL = 0.377\,\Omega$, g presents a steady state error. The latter should converge to $\overline{g} = 2V_d^2/(Rv_{S,RMS})$, i.e., $2.02\,\Omega^{-1}$ and $1.01\,\Omega^{-1}$ for $R = 10\,\Omega$ and $R = 20\,\Omega$, respectively. This steady state error is due to a DC term produced during the transformation from x_3 to z_3 which involves the square of signal x_3 containing a ripple.

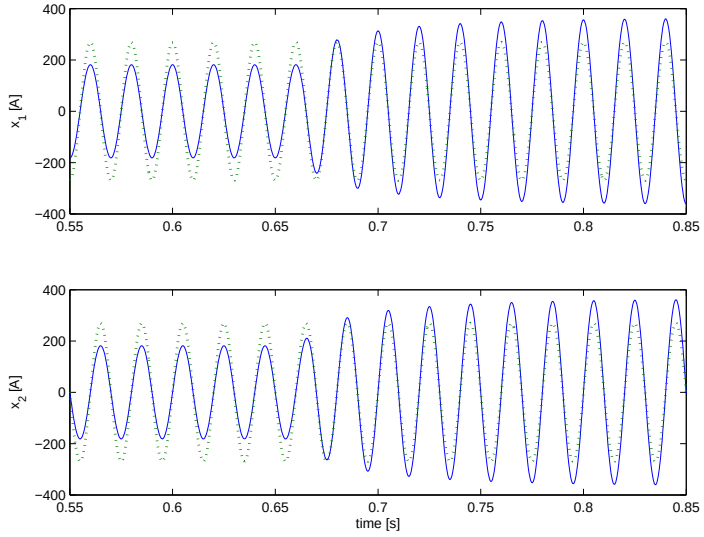

Figure 3.2: Transient response of input currents to a load step change from $20\,\Omega$ to $10\,\Omega$ at $t = 0.66$ s: **(Top)** x_1 in solid and v_{s1} in dotted line; **(Bottom)** x_2 in solid and v_{s2} in dotted line.

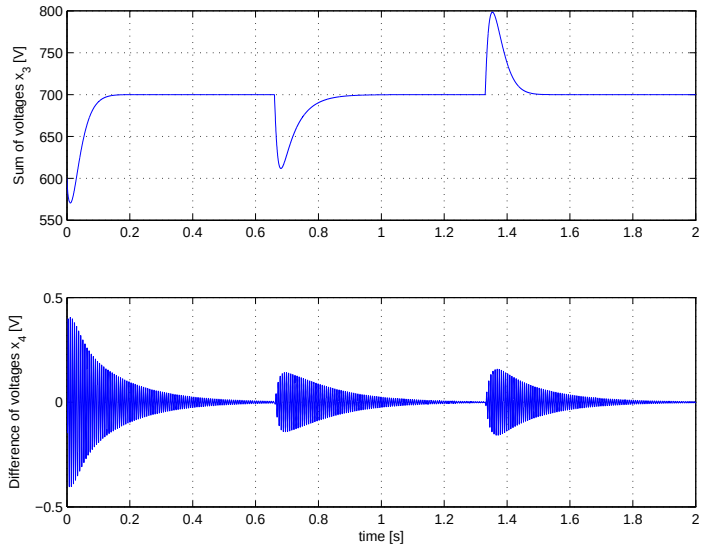

Figure 3.3: Transient response, during a load resistor change from 20Ω to 10Ω at $t = 0.66$s, and back to 20Ω at $t = 1.33$s, of: **(Top)** the sum of capacitors voltages $x_3 = v_{C1} + v_{C2}$, and **(Bottom)** the difference of capacitors voltages $x_4 = v_{C1} - v_{C2}$.

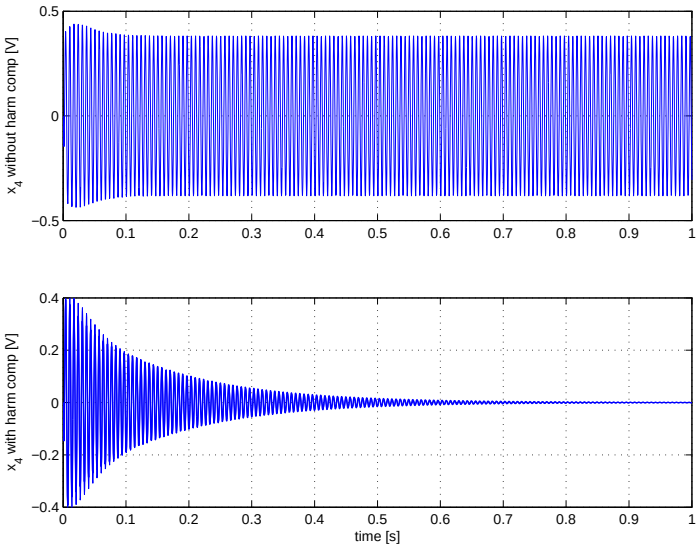

Figure 3.4: Transient response of the difference of capacitors voltages $x_4 = v_{C1} - v_{C2}$ from start up: **(Top)** without harmonic compensation, and **(Bottom)** with harmonic compensation.

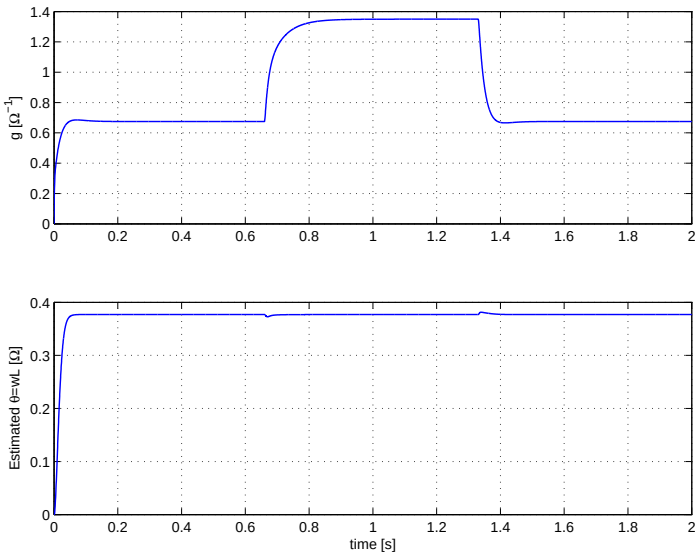

Figure 3.5: Transient response, during a load resistor change from 20Ω to 10Ω at $t = 0.66$s, and back to 20Ω at $t = 1.33$s, of: **(Top)** the gain g, and **(Bottom)** the estimate $\hat{\theta} = \widehat{wL}$.

3.5 Experimental results

In order to validate the mathematical model and show the effectiveness of the proposed controller, experimental results are shown.

For this purpose, the proposed control algorithm was programmed in a fixed-point DSP TMS320LF2407A in cascaded with a floating-point DSP VC33, for a prototype of 10kW. The following parameters have been selected: a nominal frequency of 50 Hz ($\omega_0 = 314.16$ rad/s); inductances of 3mH; capacitors of 6600μF and load of 35Ω.

Figure 3.6 shows the compensated source currents i_{S123}. It is important to point that the reference of the current is gv_S, and then, because the source voltages is not perfectly sinusoidal, the source current follows a distorted signal.

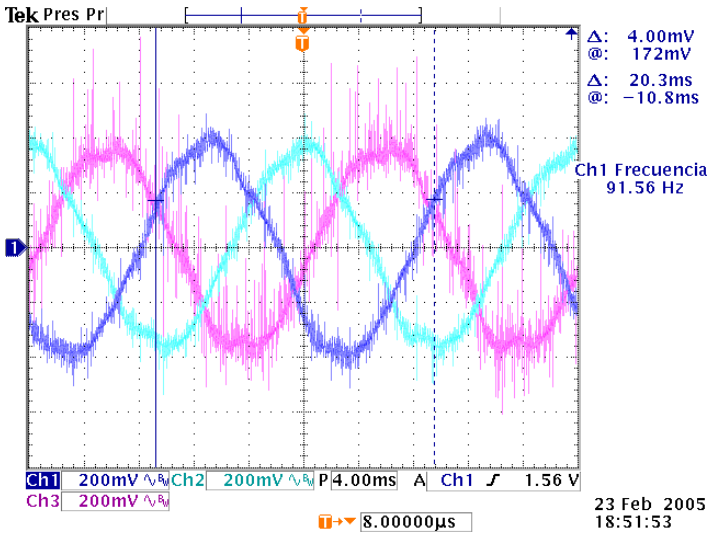

Figure 3.6: Compensated source currents i_{S123}

Figure 3.7 shows the compensated source currents i_{S123} during a load change from 1kW to 10kW (800V). The current follows the new reference in a relatively short time and the overshoot is almost imperceptible.

Figure 3.8 shows the capacitor voltages transient response when the load is changed from 1kW to 10kW (750V). It is shown that after a relatively small transient, all capacitor voltages converges towards their common reference 375V_{DC}.

Figure 3.9 shows the rectified voltage during a load change from 1kW to 10kW (800V). It is shown that after a relatively small transient, the rectifier voltage converges towards its reference 800V_{DC}.

Figure 3.10 shows the rectified voltage in a reference change from 750V to 850V. It is shown that the voltage reach the new reference after a relatively short transient.

3.6 Conclusions

In this chapter it was proposed a nonlinear controller based on a model for the three-level NPC converter just proposed in the Chapter 2 of this thesis. The main feature of this

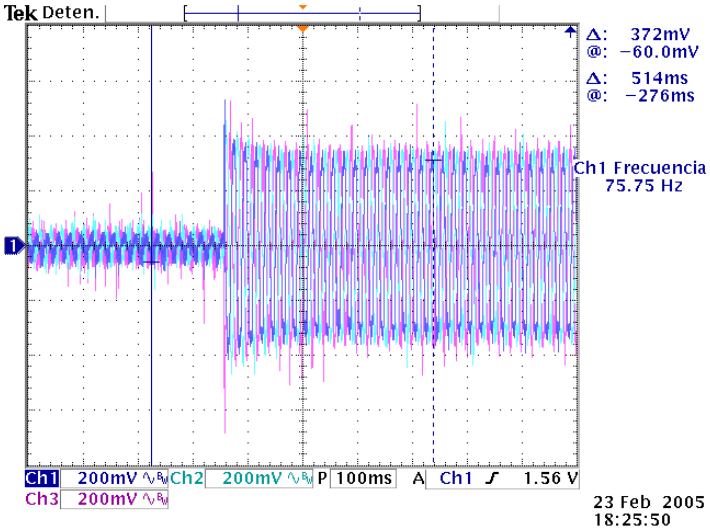

Figure 3.7: Compensated source currents i_{S123}

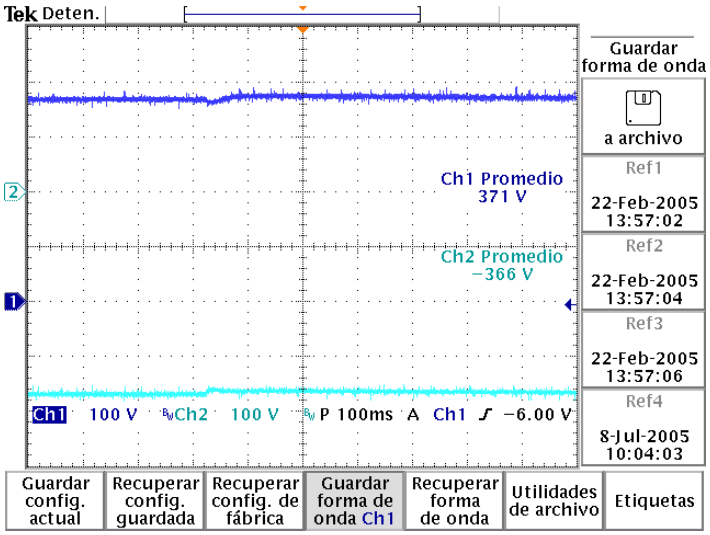

Figure 3.8: Capacitor voltages during a load change

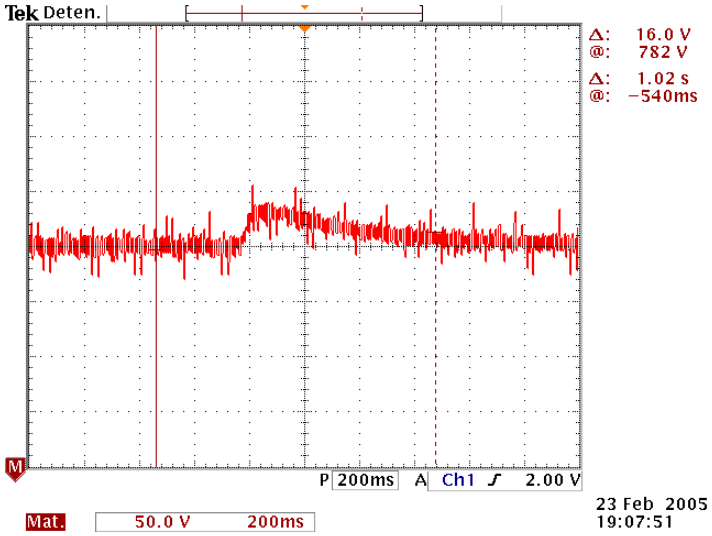

Figure 3.9: Rectified voltage during a load change from 1kW to 10kW (800V)

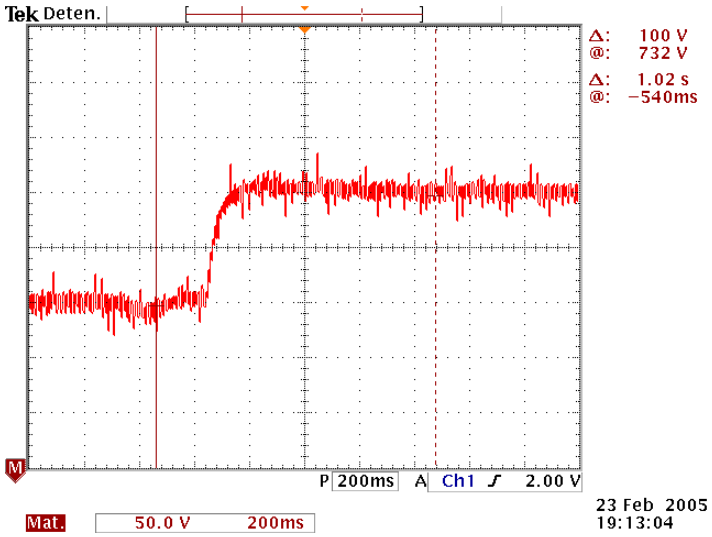

Figure 3.10: Rectified voltage in a reference change from 750V to 850V.

model was the existence of a third degree of freedom (DOF) offered by the control input, and referred as the γ-component, which represents a crucial DOF useful to deal with the balancing of the capacitors voltages. It is important to remark that in previous works, this DOF has been neglected or simply disregarded. The model was written in terms of the sum and the difference of the capacitors voltages, which were perhaps the natural variables of representation, besides the inductors currents. According to this description, it was found that the difference of the capacitors voltages, which should in principle be reduced to zero to guarantee the balancing, is indeed perturbed by higher order harmonics, mainly a third harmonic. To overcome this issue, it was included in the control design a harmonic compensation mechanism to cope with these disturbances.

The simulation results and experimental results show the effectiveness of the proposed controller. Notice that the experimental results show in the source currents a distortion with a remarkable third harmonic, this due the fact that the reference current is given by gv_S, and then, because the source voltages is not perfectly sinusoidal, the source current follows a distorted signal. Out of that, the experimental response is exactly like the simulations predicted, obviously with more distortion due the physical limitations of the prototype and the commutation losses. Moreover, the distortions in the capacitor voltages are minimum in relation with the DC voltage, and the overvoltage during the load change is minor to the 5 percent of the DC voltage, showing the controller a very good performance, even when the voltage reference is changed, reaching the desired value in a relatively short time.

Chapter 4

Modeling and Control of a Single-phase Cascade H-Bridge Multilevel Converter

4.1 Introduction

Inside the different topologies of multilevel converters, the cascade H-bridge topology is an attractive option given its different advantages such as the modularity, the simplest composition and the reduced number of components (they do not have the need of extra clamping diodes, nor balance capacitors). Even more, the structure of multicells in H-bridge allows the nourishment of different charges in DC when is used like active rectifier. In contrast with the advantages that present this type of converters, they have a major challenge regarding their control, this is due to the fact that every H-bridge cannot be considered to be an independent structure of control, but it must interact with other cells to be able to obtain a current almost sinusoidal and in phase with the line voltage on the AC side, at the same time as they must regulate and stabilize the voltages in every capacitor on the DC side.

To achieve these requirements different control techniques can be considered and the controller design can be carried out by following different criteria. An interesting technique of control that has been applied in different works is the Passivity-Based Control (PBC). The idea behind this technique is to consider the system dynamics as the sum of energy-transformation subsystems and to control their energy exchanges. The theoretical framework of the PBC can be found in [44] and some applications to multilevel converters are found in [32]. On the other hand, and even though there are several mathematical models can be found in the literature, the control techniques applied until now do not use such models for the controller design.

This chapter presents the modeling and control process of the cascade h-bridge single-phase multilevel converter used as a shunt active filter. Based on a mathematical model, a controller is proposed to guarantee a current tracking of the line current towards a reference proportional to the line voltage. Simultaneously, the controller guarantees the regulations and balance of the capacitor voltages. Crucial for the developments is the transformation of the model in terms of the sum and the difference of the squares of the capacitors voltages. Moreover, it is shown that, while the current tracking problem and the regulation problem depend on the sum of the injected voltages, the balance depends on the difference between them. The results are shown for a single-phase five-level cascade h-bridge converter as a

shunt active filter, however, can be easily extended to higher levels.

4.2 Model of the five level HB multilevel converter

In this chapter an active filter using the single-phase 5 level cascade h-bridge converter is considered. The results, however, can be easily extended to higher levels. The basic setup is shown in Fig.4.1.

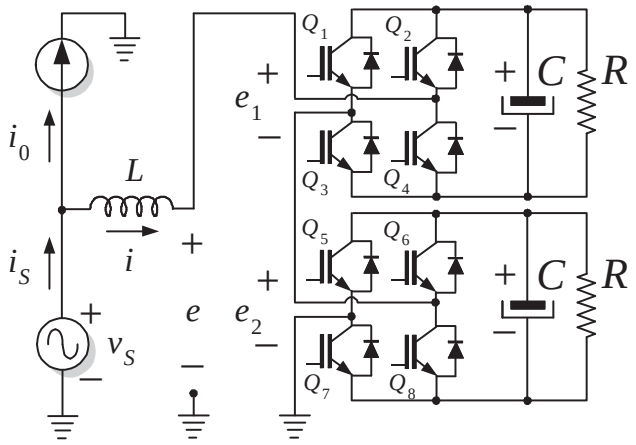

Figure 4.1: Single-phase five-level cascade h-bridge converter used as a shunt active filter.

The modeling process is divided in two stages. First, the expressions for the inductor currents dynamics are obtained, and second, the expressions that describes the capacitors voltages dynamics.

The model can be obtained by simple application of Kirchhoff's laws, this yields the system

$$
\begin{aligned}
L\frac{di}{dt} &= -u_1 v_{C1} - u_2 v_{C2} + v_S && (4.1)\\
C\frac{dv_{C1}}{dt} &= u_1 i - \frac{v_{C1}}{R} && (4.2)\\
C\frac{dv_{C2}}{dt} &= u_2 i - \frac{v_{C2}}{R} && (4.3)\\
i_S &= i + i_0 \\
e_1 &= u_1 v_{C1} \ , \ e_2 = u_2 v_{C2} \\
e &= e_1 + e_2
\end{aligned}
$$

where parameters L and C are the input inductance and DC-side capacitance of the active filter, respectively. Notice that, without loss of generality, the same capacitance C has been assumed for both h-bridges, as well as the losses represented by R; i_S is the line current, v_{C1} and v_{C2} are the capacitors voltages; $i(t)$ represents the injected active filter current; $u_1(t)$ and $u_2(t)$ denote the switch position functions for each H-bridge and act as the control inputs, which take values in the discrete set $\{-1, 0, 1\}$. For instance, for $u_1 = 1$ transistors Q_1 and

Q_4 are turned on, while transistors Q_2 and Q_3 are turned off, and the opposite for $u_1 = -1$. Moreover, for $u_1 = 0$, either, Q_1 and Q_2 are both on, or Q_3 and Q_4 are both on. The lower H-bridge operates in a similar way.

For the control design purposes the *averaged model* is considered instead, i.e., the control inputs u_1 and u_2 represent, from now on, continuous signals taking values in the range $[-1,\ 1]$. This is supported by the fact that, for the real implementation, an appropriate modulation technique, such as multi-carrier phase-shifted or level-shifted, with a relative high effective switching frequency is used.

For controller design purposes it is more convenient to transform the model above as follows

$$L\frac{dx_1}{dt} = -L\frac{di_0}{dt} - \delta_1 + v_S \tag{4.4}$$

$$C\frac{dx_2}{dt} = \delta_1 x_1 - \frac{2}{R}x_2 \tag{4.5}$$

$$C\frac{dx_3}{dt} = \delta_2 x_1 - \frac{2}{R}x_3 \tag{4.6}$$

where the following definitions have been used

$$\begin{aligned} x_1 &\triangleq i_S \\ x_2 &\triangleq \frac{v_{C1}^2 + v_{C2}^2}{2} \\ x_3 &\triangleq \frac{v_{C1}^2 - v_{C2}^2}{2} \\ \delta_1 &\triangleq u_1 v_{C1} + u_2 v_{C2} \\ \delta_2 &\triangleq u_1 v_{C1} - u_2 v_{C2} \end{aligned}$$

Notice that, the model is expressed in terms of the line current, instead of the injected current as in conventional controllers. This allows a more natural compensation of the line current, and with the benefit that, a reduced number of sensors is required. Notice that, x_2 and x_3 represent the sum and the difference, respectively, of the squares of the capacitors voltages, while δ_1 and δ_2 represent the sum and the difference of the injected voltages. These last two signals represent the actual control inputs of system (5.21)-(5.23). In fact, the original control signals can be reconstructed as $u_1 = (\delta_1 + \delta_2)/(2v_{C1})$ and $u_2 = (\delta_1 - \delta_2)/(2v_{C2})$. Notice that, all these transformations reduce considerably the model expressions.

Main assumptions:

A1. *[decoupling assumption]* It is assumed that, the inductor current dynamics are faster than the capacitor voltage dynamics. Thus based on the time scale separation principle, the control design is split in two parts, namely, an *inner (tracking) current loop* and an *outer voltage loop*.

A2. The load current i_0 and source voltage v_S are periodic signals that contain higher odd harmonics of the fundamental frequency $\omega_0 = 2\pi f_0$, which is a known constant, and

have the following Fourier series description.

$$v_S = \sum_{k\in H} \rho_k^\top V_{S,k} \tag{4.7}$$

$$i_0 = \sum_{k\in H} \rho_k^\top I_{0,k} \tag{4.8}$$

where

$$\rho_k = \begin{bmatrix} \cos(k\omega_0 t) \\ \sin(k\omega_0 t) \end{bmatrix}, \; V_{S,k} = \begin{bmatrix} V_{S,k}^r \\ V_{S,k}^i \end{bmatrix}, \; I_{0,k} = \begin{bmatrix} I_{0,k}^r \\ I_{0,k}^i \end{bmatrix}$$

numbers $I_{0,k}^r$, $I_{0,k}^i$, $V_{S,k}^r$ and $V_{S,k}^i \in \mathbb{R}$ are the k^{th} harmonic coefficients of the Fourier series description (also referred as the phasors) of the load current and source voltage, respectively. The harmonic coefficients are assumed unknown constants (or slowly varying) and $H = \{1, 3, 5, ...\}$ is the set of indexes of the considered odd harmonic components. Superscripts $(\cdot)^r$ and $(\cdot)^i$ are used to distinguish the coefficients associated to $\cos(k\omega_0 t)$ and $\sin(k\omega_0 t)$, respectively.

A3. System parameters L, C and R are unknown positive constants.

4.3 Controller design

For controller design purposes it is also assumed that the inductor current dynamics are faster than the capacitor voltage dynamics. Thus, based on the time scale separation principle, the control design is split in two parts, an inner current (tracking) control loop and an outer voltage control loop. As stated above, the dynamics of the capacitors voltages have been transformed and expressed in terms of the sum and difference of the squares of the capacitors voltages. Therefore the voltage control loop is divided in its turn in two more control loops: a *regulation loop* that forces the sum of the squares towards a desired constant value v_d^2 and, a *balance loop* to zero the difference of the squares. Notice that, under the assumption that both capacitor voltages keep a positive value, which is valid in normal operation, the fulfilment of the above regulation and balance objectives guarantee the regulation of both capacitors voltages towards the same constant reference, that is, $v_{C1} \to V_d$ and $v_{C2} \to V_d$.

4.3.1 Current tracking loop

A control signal δ_1 in (5.21) is designed to force the source current to follow a reference current signal proportional to the line voltage, that is,

$$x_1 = i_S \to i_S^* = \eta v_S / v_{S,\text{RMS}}^2$$

where i_S^* represents the current reference, with $\eta / v_{S,\text{RMS}}^2$ a scalar representing the apparent conductance observed by the source. This is equivalent to seek for an operation with power factor close to unity. In this case, the following controller is proposed

$$\delta_1 = v_S - \hat{\phi} + k_1 \tilde{x}_1 \tag{4.9}$$

where $k_1 > 0$ is a design parameter, and $\tilde{x}_1 = x_1 - x_1^*$. The expression for δ_1 cancels v_S, adds a damping term $k_1(i_S - i_S^*)$ to reinforce the stability, and finally, it includes a harmonic compensation scheme represented by $\hat{\phi}$.

This yields the following perturbed LTI system, referred as the error dynamics

$$L\dot{\tilde{x}}_1 = -k_1\tilde{x}_1 - \hat{\phi} + \phi \tag{4.10}$$

where $\phi = -L\dot{x}_1^*$, which can be considered as a periodic disturbance based on **A2**.

Following a similar adaptive approach as in [36], an expression for $\hat{\phi}$ can be proposed as follows

$$\hat{\phi} = \sum_{\ell \in H} \frac{s\gamma_\ell}{s^2 + \ell^2\omega_0^2}\tilde{x}_1 \tag{4.11}$$

where γ_ℓ, $(\ell \in H)$ is a positive design parameter. Notice that, this harmonic compensator consists on a bank of harmonic oscillators tuned at the harmonics under concern, that is, the odd harmonics, which confirms the well known *internal model principle*. This inner loop is shown in Fig.4.2. A complete stability analysis, and more details on the derivation of this part of the controller can be found in [36].

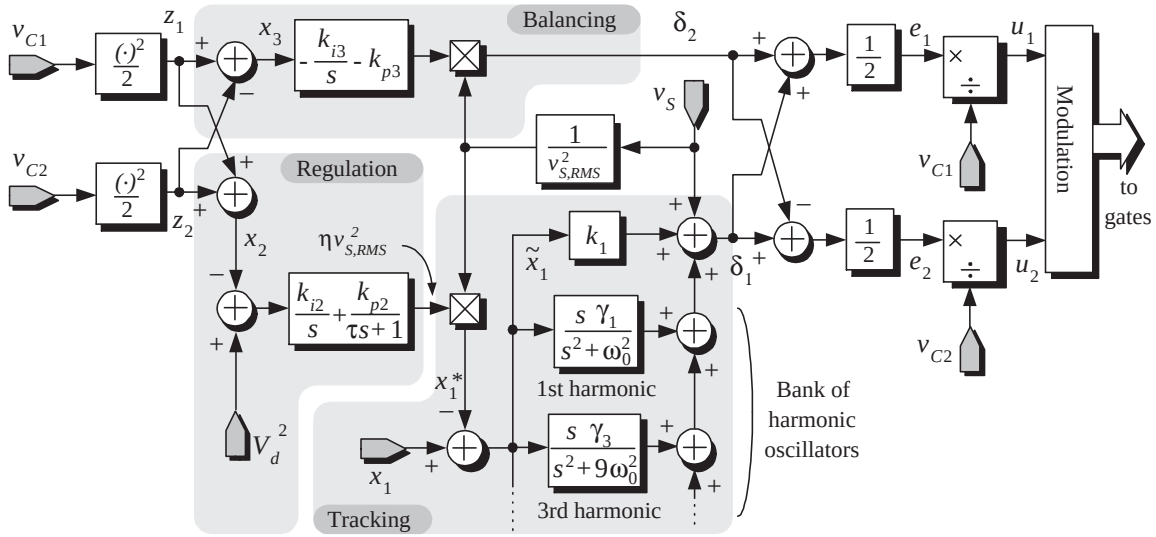

Figure 4.2: Block diagram of the overall proposed controller.

4.3.2 Regulation loop

It is designed to drive the sum of the squares of the capacitors voltages towards a desired constant reference V_d^2, that is, $x_2 \to V_d^2$. This guarantees that enough energy has been stored in both capacitors for the correct fulfillment of the previous objective. Out of this control loop, an expression for the scalar η is obtained, which is required to construct the reference i_S^* defined above. In this case, based on **A1**, it is proposed to use the traditional

proportional term of limited bandwidth plus an integral term, both operating on the error signal $\tilde{x}_2 \triangleq (x_2 - V_d^2)$, which is given below in its form of a transfer function

$$\eta = -\left(\frac{k_{i2}}{s} + \frac{k_{p2}}{\tau s + 1}\right)\tilde{x}_2 \tag{4.12}$$

where k_p, k_i are the proportional and integral gains of a PI controller, respectively, and τ the time constant of a low-pass filter (LPF) affecting the proportional term. This controller guarantees that, $x_2 \rightarrow V_d^2$ in average, with η bounded. The regulation loop is shown in Fig.4.2.

4.3.3 Balance loop

Finally, an expression for the control signal δ_2 is designed to zero the difference of the squares of the capacitors voltages. Based on **A1**, it can be considered that, after a relatively small time, $x_1 = x_1^*$, therefore subsystem (5.23) can be rewritten as

$$C\dot{x}_3 = \delta_2 \frac{\eta v_S}{v_{S,\text{RMS}}^2} - \frac{2}{R}x_3 \tag{4.13}$$

In this case, the following controller is proposed

$$\delta_2 = -\xi \frac{v_S}{v_{S,\text{RMS}}^2} \tag{4.14}$$

$$\xi = k_{p3}x_3 + k_{i3}\psi \ , \ \dot{\psi} = x_3 \tag{4.15}$$

The expression of controller δ_2 consists on a signal proportional to the line voltage v_S whose amplitude is modulated by a proportional plus integral scheme operating on the difference of the squares x_3. Notice that, another proposal could be $\delta_2 = \xi v_S/(v_{S,\text{RMS}}^2\eta)$, that is, including a division by η. However, it was observed during implementation that, this controller increased the control effort and did not improve substantially the performance.

The proposed control guarantees that, $x_3 \rightarrow 0$ in average, as can be confirmed in the following model

$$C\frac{dx_3}{dt} = -(\eta k_{p3} + \frac{2}{R})x_3 - \eta k_{i3}\psi \tag{4.16}$$

$$\dot{\psi} = x_3 \tag{4.17}$$

which is an approximation of the DC component of x_3 dynamics[1]. Notice that, in normal operation η is a positive bounded variable. The balance loop is shown in Fig.4.2.

4.4 Numerical results

Numerical simulations using PSCAD 4.0 have been carried out. A voltage source of 127V_{RMS}, f_0=60Hz (w_0=377rad/s) is considered. A diode bridge rectifier with a resistive

[1]The extraction of the the dc component of a scalar x is defined, at time t, by the following averaging operation $\langle x\rangle_0(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)d\tau$, referred also as the moving average.

load of either 40Ω or 20Ω, and a bulky capacitor of 100μF is considered as the nonlinear load. This load produces a distorted current containing all odd harmonics of the fundamental frequency (60Hz). The active filter has been designed with parameters $L = 0.7$mH, $C = 4400\,\mu$F, $R = 10$ kΩ. The switching frequency for the switching devices is fixed to 15kHz. The control parameters are fixed to $k_1 = 7$, $k_{p2} = 0.288$, $k_{i2} = 0.0216$, $k_{p3} = 0.1286$, $k_{i3} = 0.2857$. The set of compensated harmonics are $\{1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23\}$ with gains $\gamma_1 = 150$, $\gamma_3 = 190$, $\gamma_5 = 210$, $\gamma_7 = 230$, $\gamma_9 = 210$, $\gamma_{11} = 220$, $\gamma_{13} = 230$, $\gamma_{15} = 240$, $\gamma_{17} = 250$, $\gamma_{19} = 260$, $\gamma_{21} = 270$, $\gamma_{23} = 280$.

Figure 4.3 shows the transient responses observed during a load step change. For this, the load resistor in the diode rectifier is changed from 40 Ω to 20 Ω. It is shown that, the compensated source current $i_S(t)$ (top plot) is an almost sinusoidal signal in phase with the source voltage $v_S(t)$, despite of the highly distorted load current $i_0(t)$ (medium plot). In the bottom plot the injected current $i(t)$ is presented.

Figure 4.4 shows the capacitors voltages transient responses during start-up and when the load in the diode bridge rectifier is changed from 40 Ω to 20 Ω. It is shown that, after a relatively small transient, the capacitors voltages $v_{C1}(t)$ and $v_{C2}(t)$ converge towards their reference fixed at 110 V for both. This figure also shows that, the apparent conductance $\eta(t)/v_{S,\text{RMS}}^2$ reaches, after a slight transient, a constant value proportional to the power dissipated by the load.

Figure 4.5 shows the injected voltage e as computed in the control algorithm (in gray) and the resulting modulated signal using the multicarrier phase-shifted modulation algorithm. Finally, Fig. 4.6 shows that, the total harmonic distortion (THD) of the compensated current i_S decreases from 8% for the lowest load (40 Ω) to 5% for the highest load (20 Ω).

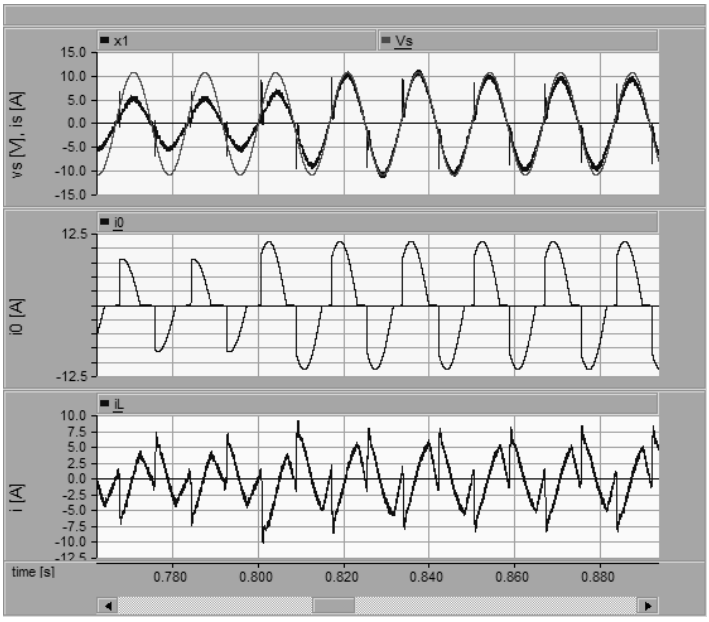

Figure 4.3: **(from top to bottom)** Transient responses of line voltage $v_S(t)$, compensated current $i_S(t)$, load current $i_0(t)$, and injected current $i(t)$ during a load step change.

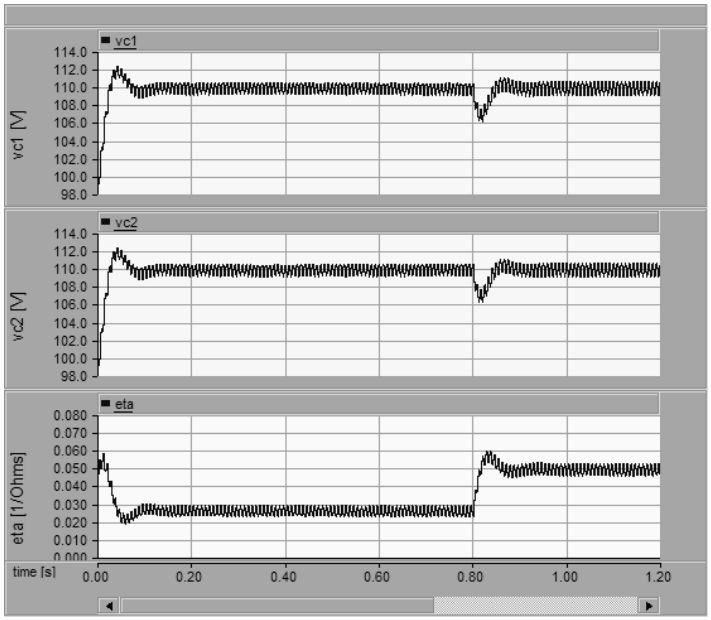

Figure 4.4: **(from top to bottom)** Transient responses of the capacitor voltages $v_{C1}(t)$ and $v_{C2}(t)$, and apparent conductance $\eta(t)$ observed by the source at start-up and during a load change.

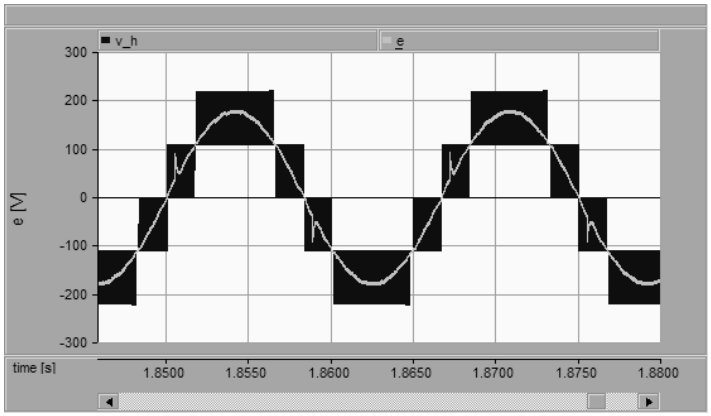

Figure 4.5: **(gray)** Injected voltage e as computed in the control algorithm, and **(black)** the real injected voltage e using a multicarrier phase-shifted modulation algorithm.

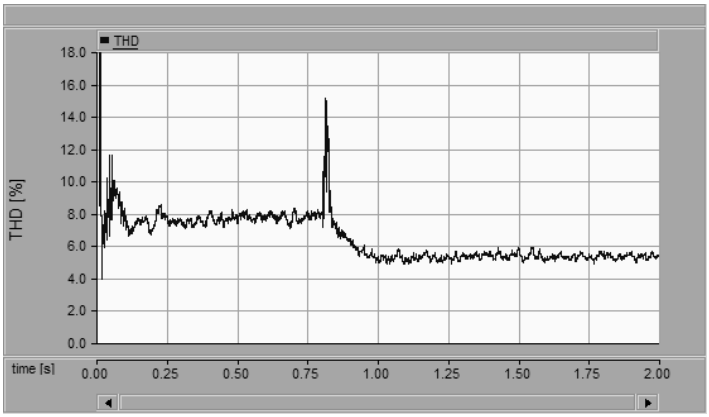

Figure 4.6: THD of the compensated current i_S at start-up and during a load change.

4.5 Some preliminary experimental results

Experimental results using a DSP2407 controlling a prototype are presented. These results are preliminary because it was found that it is necessary to program the proposed controller in a DSP with more computational capacity in order to obtain better experimental results.

A voltage source of 127V_{RMS}, f_0=60Hz (w_0=377rad/s) is considered. A diode bridge rectifier with a resistive load of either 35Ω or 70Ω, and a bulky capacitor of 100μF is considered as the nonlinear load. This load produces a distorted current containing all odd harmonics of the fundamental frequency (60Hz). The active filter has been designed with parameters $L = 3$mH, $C = 2200\,\mu$F, $R = 22000\,\text{k}\Omega$. The switching frequency for the switching devices is fixed to 15kHz. The control parameters are fixed to $k_1 = 7$, $k_{p2} = 0.288$, $k_{i2} = 0.0216$, $k_{p3} = 0.1286$, $k_{i3} = 0.2857$. The DC voltage reference was settled at 50V.

Figure 4.7 shows the transient response observed during a start-up. The figure shows, from top to bottom, both capacitor voltages reaching the desired value of 50V, the converter injected voltage with five staggered levels and the source current.

Figure 4.8 shows the capacitor voltages reaching the reference of 50V, the injected voltage and the source current.

Figure 4.9 shows the capacitor voltages (TOP), the injected voltage and the source current in phase with the source voltage (in black).

Figure 4.10 shows the injected voltage e as computed in the control algorithm (in black) and the resulting modulated signal using the multicarrier phase-shifted modulation algorithm. It is also shown the capacitor voltages (TOP) and the source current (BOTTOM).

4.6 Conclusions

In this chapter it was presented the modeling and control for the cascade H-bridge single-phase multilevel converter used as a shunt active filter. Based on the proposed mathematical model, a controller was designed to guarantee a current tracking of the line current towards

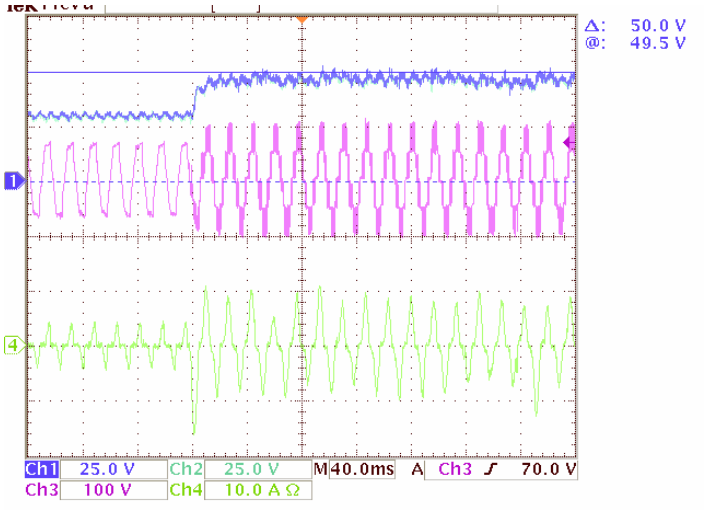

Figure 4.7: Transient response observed during a start-up. The figure shows, from top to bottom, both capacitor voltages, the converter output voltage and the source current.

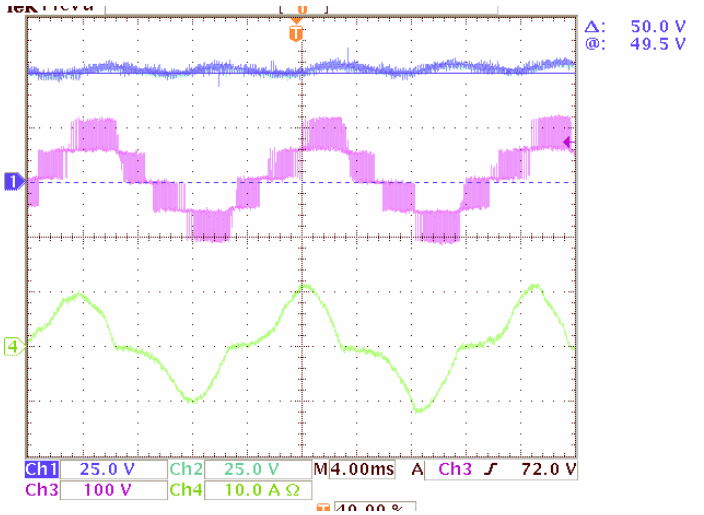

Figure 4.8: From top to bottom, both capacitor voltages, the converter output voltage and the source current.

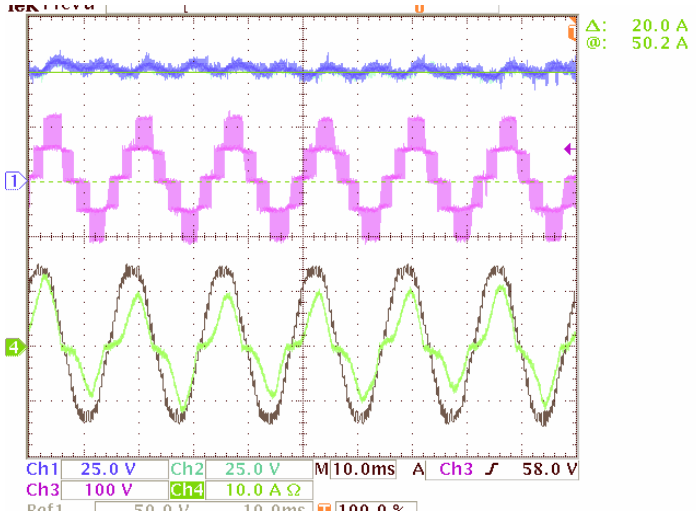

Figure 4.9: shows the capacitor voltages (TOP), the injected voltage and the source current in phase with the source voltage (in black).

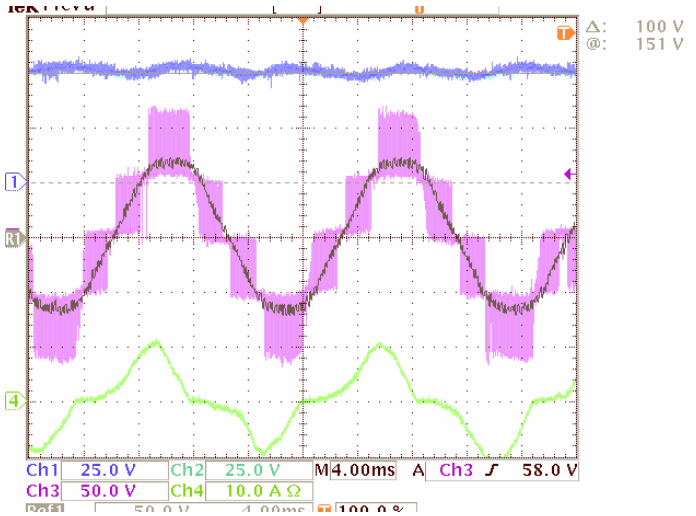

Figure 4.10: From top to bottom, the capacitor voltages, the injected voltage e as computed in the control algorithm (in black) and the resulting modulated signal using the multicarrier phase-shifted modulation algorithm, and the source current.

a reference proportional to the line voltage. In addition, the controller guaranteed the regulations and balance of the capacitor voltages. Crucial for the developments was the transformation of the model in terms of the sum and the difference of the squares of the capacitors voltages. In fact, it was shown that, while the current tracking problem and the regulation problem depend on the sum of the injected voltages, the balance depends on the difference between them.

The preliminary experimental results shows a response almost identical to the simulations results, and although the computational limitation of the DSP, the proposed controller allows the balancing of the voltages of the capacitors and reach the desired DC voltage value. These results provide a basis to believe that with more computational capacity, the results will be the predicted in the simulations.

Chapter 5

Modeling and Control of a Three-phase Five-level Cascade H-Bridge Multilevel Converter

5.1 Introduction

As mentioned before, one of the major challenges in this type of converters is the control design. In effect, such a controller must be able to guarantee stable regulation of the voltages of every single capacitor on the DC side, all this in addition to the usual current tracking control on the AC side. However, in these converters, the number of available controllers is inferior to the controlled variables. For instance, in a three-phase H-bridge converter of $2n + 1$ levels (n H-bridge converters in cascade), the control problem consists in controlling $n + 3$ state variables (three currents plus n DC voltages) with only n switching functions. This is due to the fact that every H-bridge cannot be considered as an independent structure to control, as they interact with other cells. For instance, in a branch of a series connection of H-bridges they share the same current and the effective injected voltage is the sum of voltages in every cell.

For the three-phase multilevel cascade converter there are a few proposed solutions very ingenious and intuitive, but in most cases there is a lack of formalism, and as mentioned above, they are not model based. One big issue that has bee observed is that, with the explicit available controllers it seems like the desired equilibrium point is inadmissible [46].

Generally speaking, an active filter application involves the compensation of harmonic distortion and reactive power, i.e., periodic disturbances, caused by a distorting nonlinear load. Control schemes based on the introduction of a bank of harmonic oscillators (resonant filters) is perhaps one of the most appealed techniques to guarantee rejection of periodic disturbances, thanks to its simplicity and effectiveness. This type of schemes is based on the internal model principle. This principle states that the controlled output can track a class of reference commands without a steady state error if the generator, or the model, of the reference is included in the stable closed-loop system. Therefore, according to the internal model principle, if a periodic disturbance has an infinite Fourier series (of harmonic components), then an infinite number of resonant filters are required to reject such a disturbance.

This chapter presents a mathematical model for cascade H-bridge three-phase multilevel

converter used as a shunt active filter. Based on the model, a controller is proposed in order to achieve the requirements of the system, that is, to compensate harmonic distortion and reactive power due to a nonlinear load. This is accomplished by guaranteeing that the line current follows a reference proportional to the line voltage during the steady state. Additionally, the controller guarantees regulation and balance of the capacitors voltages. The transformation of the model in terms of the sum and the difference of the squares of the capacitors voltages is crucial for our developments. The idea behind the controller is the introduction of certain amount of distortion during the transient, which permits the balancing of the capacitors voltages. It is shown that, once the balancing is reached, this distortion vanishes, thus remaining a current reference proportional to the source voltage in the steady state. After suitable transformations to the model, it is shown that the natural control inputs are the sum and the difference of the so called injected voltages. Moreover, it is shown that, while the current tracking problem and the regulation problem depend on the sum of the injected voltages, the balance depends on the difference between them. The three-phase five-level topology is studied here, however, the results can be easily scaled to higher levels.

5.2 System description

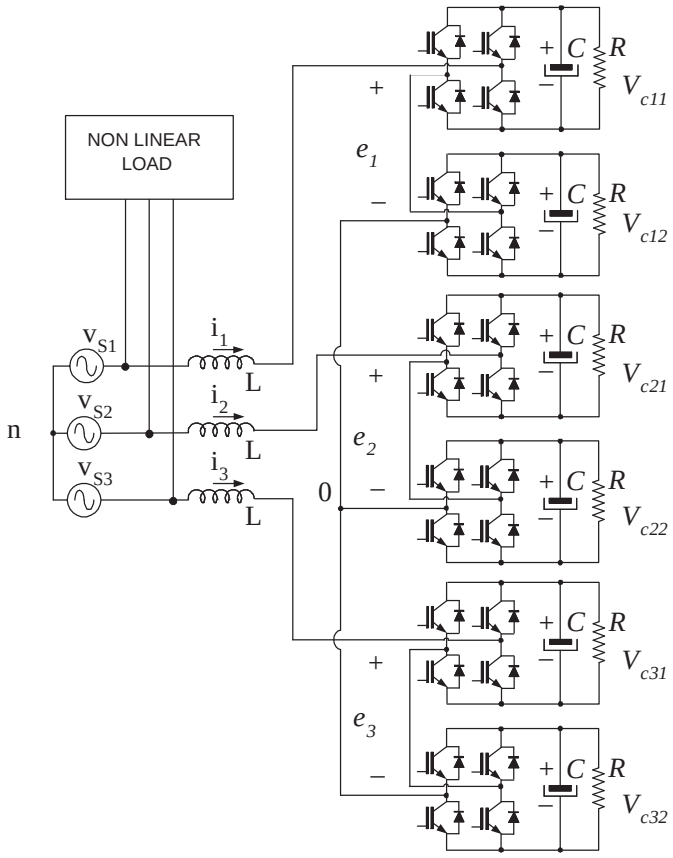

Figure 5.1: Three-phase five-level cascade H-bridge converter.

In this chapter, an active filter using three-phase five-level cascade H-bridge converter shown in Fig.5.1 is considered. The model can be obtained by simple application of Kirchhoff's laws, which yields the system

$$
\begin{aligned}
L\frac{d}{dt}i_{S1} &= v_{S1} - (e_{11}+e_{12}) - v_{0n} + L\frac{d}{dt}i_{01} && (5.1)\\
L\frac{d}{dt}i_{S2} &= v_{S2} - (e_{21}+e_{22}) - v_{0n} + L\frac{d}{dt}i_{02} && (5.2)\\
L\frac{d}{dt}i_{S3} &= v_{S3} - (e_{31}+e_{32}) - v_{0n} + L\frac{d}{dt}i_{03} && (5.3)\\
C\frac{d}{dt}z_{11} &= e_{11}(i_{S1}-i_{01}) - \frac{2z_{11}}{R} && (5.4)\\
C\frac{d}{dt}z_{12} &= e_{12}(i_{S1}-i_{01}) - \frac{2z_{12}}{R} && (5.5)\\
C\frac{d}{dt}z_{21} &= e_{21}(i_{S2}-i_{02}) - \frac{2z_{21}}{R} && (5.6)\\
C\frac{d}{dt}z_{22} &= e_{22}(i_{S2}-i_{02}) - \frac{2z_{22}}{R} && (5.7)\\
C\frac{d}{dt}z_{31} &= e_{31}(i_{S3}-i_{03}) - \frac{2z_{31}}{R} && (5.8)\\
C\frac{d}{dt}z_{32} &= e_{32}(i_{S3}-i_{03}) - \frac{2z_{32}}{R} && (5.9)
\end{aligned}
$$

$$
\begin{aligned}
e_{11} &= u_{11}v_{C11} \ , \ e_{12} = u_{12}v_{C12}\\
e_{21} &= u_{21}v_{C21} \ , \ e_{22} = u_{22}v_{C22}\\
e_{31} &= u_{31}v_{C31} \ , \ e_{32} = u_{32}v_{C32}\\
z_{11} &= \frac{v_{C11}^2}{2} \ , \ z_{12} = \frac{v_{C12}^2}{2}\\
z_{21} &= \frac{v_{C21}^2}{2} \ , \ z_{22} = \frac{v_{C22}^2}{2}\\
z_{31} &= \frac{v_{C31}^2}{2} \ , \ z_{32} = \frac{v_{C32}^2}{2}
\end{aligned}
$$

where parameters L and C are the input inductance and dc-side capacitance of the active filter, respectively; i_{S1}, i_{S2} and i_{S3} are the line currents, i_{01}, i_{02} and i_{03} are the load currents, i_1, i_2 and i_3 are the injected currents, v_{C11}, v_{C12}, v_{C21}, v_{C22}, v_{C31} and v_{C32} are the capacitors voltages; u_{11}, u_{12}, u_{21}, u_{22}, u_{31}, and u_{32} denote the switch position functions for each H-bridge and act as the control inputs, which take values in the discrete set $\{-1, 0, 1\}$. For instance, if $u_{11} = 1$ then transistors Q_1 and Q_4 are turned on while transistors Q_2 and Q_3 are turned off, and the opposite for $u_{11} = -1$. Moreover, for $u_{11} = 0$, either, Q_1 and Q_2 are both on, or Q_3 and Q_4 are both on. The other H-bridges operates in a similar way.

Notice that, without loss of generality, the same inductance L, capacitance C and losses represented by R have been assumed for all H-bridges. As L is the same for each branch, and assuming $v_{S1} + v_{S2} + v_{S3} = 0$, then the following holds

$$
v_{0n} = -\frac{(e_{11}+e_{12}) + (e_{21}+e_{22}) + (e_{31}+e_{32})}{3} \qquad (5.10)
$$

where v_{0n} represents the voltage measured from point "0" to "n".

For the control design purpose, the *average model* is considered, i.e., the control inputs $u_{ij}, \forall i \in \{1,2,3\}$ and $\forall j \in \{1,2\}$ represent, from now on, continuous signals taking values in the range $[-1,\ 1]$, which are used later in a modulation algorithm to generate the switching sequence. This is supported by the fact that, for the real implementation, an appropriate modulation technique with a relative high switching frequency is used.

5.3 Model transformation

A first convenient transformation to the above presented model is the following

$$L\frac{d}{dt}\mathbf{i}_{S123} = \mathbf{v}_{S123} - \mathbf{B}\mathbf{e}_{123} + L\frac{d}{dt}\mathbf{i}_{0123} \tag{5.11}$$

$$C\frac{d}{dt}z_1 = e_1(i_{S1} - i_{01}) - \frac{2z_1}{R} \tag{5.12}$$

$$C\frac{d}{dt}z_2 = e_2(i_{S2} - i_{02}) - \frac{2z_2}{R} \tag{5.13}$$

$$C\frac{d}{dt}z_3 = e_3(i_{S3} - i_{03}) - \frac{2z_3}{R} \tag{5.14}$$

$$C\frac{d}{dt}y_1 = \delta_1(i_{S1} - i_{01}) - \frac{2y_1}{R} \tag{5.15}$$

$$C\frac{d}{dt}y_2 = \delta_2(i_{S2} - i_{02}) - \frac{2y_2}{R} \tag{5.16}$$

$$C\frac{d}{dt}y_3 = \delta_3(i_{S3} - i_{03}) - \frac{2y_3}{R} \tag{5.17}$$

where it has been defined

$$\begin{aligned}
e_1 &= e_{11} + e_{12}\ ,\ e_2 = e_{21} + e_{22}\ ,\ e_3 = e_{31} + e_{32} \\
\delta_1 &= e_{21} - e_{22}\ ,\ \delta_2 = e_{11} - e_{12}\ ,\ \delta_3 = e_{31} - e_{32} \\
z_1 &= z_{11} + z_{21}\ ,\ z_2 = z_{21} + z_{22}\ ,\ z_3 = z_{31} + z_{32} \\
y_1 &= z_{11} - z_{21}\ ,\ y_2 = z_{21} - z_{22}\ ,\ y_3 = z_{31} - z_{32}
\end{aligned}$$

where $\mathbf{i}_{S123} = [i_{S1}, i_{S2}, i_{S3},]^\top$ is the vector of source currents, $\mathbf{i}_{0123} = [i_{01}, i_{02}, i_{03},]^\top$ is the vector of load currents, $\mathbf{v}_{S123} = [v_{S1}, v_{S2}, v_{S3},]^\top$ is the vector of source voltages and $\mathbf{e}_{123} = [e_1, e_2, e_3,]^\top$ is the vector of injected voltages, and

$$\mathbf{B} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix}$$

Notice that, the model is expressed in terms of the line currents, instead of the injected currents. Moreover, the model (5.12)-(5.17) represents the dynamics of the sum and difference of the squares of the capacitor voltages which seems to be the natural state variables of the system.

The proposed solution requires the transformation of the equations (5.11)-(5.14) into conventional $\alpha\beta$-coordinates. For this purpose, the following transformation is used

$$\begin{bmatrix} \xi_\alpha \\ \xi_\beta \\ \xi_\gamma \end{bmatrix} = T \begin{bmatrix} \xi_1 \\ \xi_2 \\ \xi_3 \end{bmatrix} \tag{5.18}$$

The transformation matrix T used is defined as

$$T \triangleq \frac{2}{\sqrt{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

where $T^{-1} = \frac{1}{2}T^\top$, $TT^{-1} = \mathcal{I}_3$ and $\mathcal{I}_3$ is the 3×3 identity matrix.

Remark 5.1 The γ coordinate disappears because the fact that $(i_1 + i_2 + i_3) = 0 \Rightarrow i_\gamma \equiv 0$ and $(v_{S1} + v_{S2} + v_{S3}) = 0 \Rightarrow v_{S\gamma} \equiv 0$. □

Moreover, it is proposed to use the following transformations that reduce the model and reveal a structure more convenient for control design purposes.

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & -\sqrt{3} & \sqrt{3} \\ 2 & -1 & -1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} \tag{5.19}$$

Thus, after the above transformations the final expression for the model takes the form

$$L\frac{d}{dt}\mathbf{i}_{S\alpha\beta} = \mathbf{v}_{S\alpha\beta} - \mathbf{e}_{\alpha\beta} + L\frac{d}{dt}\mathbf{i}_{0\alpha\beta} \tag{5.20}$$

$$C\dot{x}_1 = \mathbf{e}_{\alpha\beta}^\top \mathbf{M}_1(\mathbf{i}_{S\alpha\beta} - \mathbf{i}_{0\alpha\beta}) - \frac{2x_1}{R} \tag{5.21}$$

$$C\dot{x}_2 = \mathbf{e}_{\alpha\beta}^\top \mathbf{M}_2(\mathbf{i}_{S\alpha\beta} - \mathbf{i}_{0\alpha\beta}) - \frac{2x_2}{R} \tag{5.22}$$

$$C\dot{x}_3 = \mathbf{e}_{\alpha\beta}^\top \mathbf{M}_3(\mathbf{i}_{S\alpha\beta} - \mathbf{i}_{0\alpha\beta}) - \frac{2x_3}{R} \tag{5.23}$$

$$C\dot{y}_1 = \delta_1(i_{S1} - i_{01}) - \frac{2y_1}{R} \tag{5.24}$$

$$C\dot{y}_2 = \delta_2(i_{S2} - i_{02}) - \frac{2y_2}{R} \tag{5.25}$$

$$C\dot{y}_3 = \delta_3(i_{S3} - i_{03}) - \frac{2y_3}{R} \tag{5.26}$$

where it has been defined

$$\mathbf{M}_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad \mathbf{M}_2 = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}, \quad \mathbf{M}_3 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Based on this model the *control objective* can be stated as follows:

(i) Tracking: Consists in forcing the source currents to track references which, in the steady state, are proportional to the corresponding source voltages, that is,

$$\mathbf{i}_{S\alpha\beta} \rightarrow \mathbf{i}^*_{S\alpha\beta}$$

where the current reference $\mathbf{i}^*_{S\alpha\beta}$ is designed according to

$$\mathbf{i}^*_{S\alpha\beta} = g_1\mathbf{M}_1\mathbf{v}_{S\alpha\beta} + g_2\mathbf{M}_2\mathbf{v}_{S\alpha\beta} + g_3\mathbf{M}_3\mathbf{v}_{S\alpha\beta}$$

where g_1 representing the apparent conductance observed by the source, and g_2 and g_3 two extra inputs required for the regulation and balancing objectives. These extra control inputs will be defined in the voltage regulation loop.

Notice that the form of this current reference is based on the structure of the transformed model. This is perhaps one of the main contributions of the present paper. The idea behind this proposal is that, once the current tracking is reached, and as a result of the projections in (5.21)-(5.23), there will appear a control input (g_1, g_2 or g_3) associated to each equation (5.21)-(5.23), which allows full controllability of this subsystem.
(ii) Regulation: All sums of the squares of capacitors voltages should be regulated to a given constant level, that is

$$z_1 \rightarrow V_d^2,\ z_2 \rightarrow V_d^2,\ z_3 \rightarrow V_d^2$$

which is equivalent to guarantee that

$$x_1 \rightarrow 3V_d^2\ \ ,\ \ x_2 \rightarrow 0\ \ ,\ \ x_3 \rightarrow 0$$

The *(iii) Balancing*: Consists in zeroing the difference of the capacitor voltages, that is,

$$y_1 \rightarrow 0\ \ ,\ \ y_2 \rightarrow 0\ \ ,\ \ y_3 \rightarrow 0$$

5.3.1 Main assumptions

A1. To make the controller robust against parameters uncertainties, the system parameters L, C and R are considered as uncertain constants, possibly changing in steps, or that can be slowly varying.

A2. To facilitate the design, it is assumed that the source voltage $\mathbf{v}_{S\alpha\beta}$ and the load current $\mathbf{i}_{0\alpha\beta}$ are unbalanced periodic signals that contain higher odd harmonics of the known fundamental frequency denoted by ω_0. That is, they can be represented as sums of harmonic components of both positive and negative sequences as follows

$$\mathbf{v}_{S\alpha\beta} = \sum_{\ell\in\mathcal{H}} \left(\boldsymbol{e}^{\mathcal{J}\ell\omega_0 t}\mathbf{V}^p_{S,\ell} + \boldsymbol{e}^{-\mathcal{J}\ell\omega_0 t}\mathbf{V}^n_{S,\ell}\right) \tag{5.27}$$

$$\mathbf{i}_{0\alpha\beta} = \sum_{\ell\in\mathcal{H}} \left(\boldsymbol{e}^{\mathcal{J}\ell\omega_0 t}\mathbf{I}^p_{0,\ell} + \boldsymbol{e}^{-\mathcal{J}\ell\omega_0 t}\mathbf{I}^n_{0,\ell}\right) \tag{5.28}$$

where $\mathbf{e}^{\mathcal{J}\ell\omega_0 t}$ is a rotation matrix of the form

$$e^{\mathcal{J}\ell\omega_0 t} = \begin{bmatrix} \cos(\ell\omega_0 t) & -\sin(\ell\omega_0 t) \\ \sin(\ell\omega_0 t) & \cos(\ell\omega_0 t) \end{bmatrix} \ , \ \mathcal{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$$

The vectors $\mathbf{V}^p_{S,\ell}$ and $\mathbf{V}^n_{S,\ell} \in \Re^2$ are the k-th harmonic coefficients for positive, negative sequences representation of the source voltage, while $\mathbf{I}^p_{0,\ell}$ and $\mathbf{I}^n_{0,\ell} \in \Re^2$ are the corresponding k-th harmonic coefficients for the load current; $\mathcal{H} = \{1, 3, 5, ...\}$. The source voltage harmonic coefficient are assumed to be unknown constants, or slowly varying signals.

A3. [Decoupling assumption] It is also assumed that, the current dynamics respond much faster than the capacitor dynamics. This simplifies the control design as, based on a scale separation principle, it can be split in a fast current tracking loop and a couple of slow voltage loops.

The control design is split in two parts. First, an inner current (tracking) control loop in which the currents provided by the source are forced to track references which are proportional to the source voltages. Second, an outer voltage control loop, which is divided in two more control loops: a regulation loop that drives the sum of the squares of the capacitor voltages of each branch towards a desired constant value and, a balance loop to force to zero the difference of the squares of the capacitor voltages of each branch. It is shown that, under the assumption that all capacitor voltages maintain a positive value, which is valid in normal operation, the fulfillment of the above control objectives guarantees the regulation of all capacitor voltages towards their constant reference independently. The complexity of the controller is also reduced as will become clear later.

5.4 Control design

For the tracking objective a control input is built which cancels measurable disturbances (such as the source voltage) adds a damping term and introduces a bank of resonant filters tuned at the selected harmonics under compensation, i.e., odd harmonics, to cancel the periodic disturbance. Controllers with this similar structure can be found in the literature as resonant regulator [37], stationary frame generalized integrator [39], multi-resonant controller [40], etc.

As described in more detail below, balancing was possible after the introduction of extra control inputs that intentionally distort the current reference. However, this distortion lasts during transients only, and vanishes in the stationary state. Based on this idea, a current reference is designed which comprises a linear combination of vectors of periodic signals with different phase shifts and possibly different sequences. Each of these signals having an associated multiplying gain, namely, g_1, g_2, g_3. In particular, the first gain g_1 is associated to a vector signal proportional to the source voltage. Therefore, it must be guaranteed that gain g_1 reaches a non zero constant value in the stationary state, while the other two gains g_2 and g_3 causing the distortion vanish. The definition of the current reference in this way constitutes the main contribution of this work.

The regulation objective is solved by designing g_1, g_2 and g_3 which are required to construct the current reference. These control loops are formed by proportional plus integral schemes operating on the corresponding error signal.

5.4.1 Current tracking loop

For the tracking objective a control input $\mathbf{e}_{\alpha\beta}$ is built based on the energy shaping plus damping injection methodology of the PBC [44]. The process consists in, first, making a copy of the subsystem representing the current dynamics and evaluate it at the desired current reference. Second, add a required damping term. Out of this the following expression is obtained

$$L\frac{d}{dt}\mathbf{i}^*_{S\alpha\beta} = \mathbf{v}_{S\alpha\beta} - \mathbf{e}_{\alpha\beta} + L\frac{d}{dt}\mathbf{i}_{0\alpha\beta} + k_1\tilde{\mathbf{i}}_{S\alpha\beta}$$

where $\tilde{\mathbf{i}}_{S\alpha\beta} = \mathbf{i}_{S\alpha\beta} - \mathbf{i}^*_{S\alpha\beta}$, $k_1 > 0$.

This subsystem is then solved for $\mathbf{e}_{\alpha\beta}$, which yields the controller expression

$$\mathbf{e}_{\alpha\beta} = k_1\tilde{\mathbf{i}}_{S\alpha\beta} + \mathbf{v}_{S\alpha\beta} + \boldsymbol{\phi}$$

where $\boldsymbol{\phi} = L\frac{d}{dt}\left(\mathbf{i}_{0\alpha\beta} - \mathbf{i}^*_{S\alpha\beta}\right)$. Notice that $\boldsymbol{\phi}$ represents an unknown periodic disturbance. Compensation of this type of disturbances has been addressed using different schemes, where the most appealed are based on the use of the Internal Model Principle [47]. This technique consists in the introduction of either a bank of resonant filters tuned at the harmonics under compensation (see [48] and the references therein) or a repetitive scheme (see [49] and [50] and the references therein) to compensate for such a periodic disturbance. In this case the following controller for the current tracking loop is proposed

$$\begin{aligned}\mathbf{e}_{\alpha\beta} &= k_1\tilde{\mathbf{i}}_{S\alpha\beta} + \mathbf{v}_{S\alpha\beta} + \\ &+ \sum_{k\in\mathcal{H}} \text{diag}\left\{\frac{2\gamma_k s}{s^2+k^2\omega^2}, \frac{2\gamma_k s}{s^2+k^2\omega^2}\right\}\tilde{\mathbf{i}}_{S\alpha\beta}\end{aligned} \tag{5.29}$$

where γ_k, $\forall k \in \mathcal{H}$, are positive design parameters, and s is the Laplace complex variable. Basically, the proposed controller cancels $\mathbf{v}_{S\alpha\beta}$, adds a damping term of the form $k_1\tilde{\mathbf{i}}_{S\alpha\beta}$ and includes a bank of resonant filters tuned at the harmonics of interest (odd) for harmonic compensation.

Controllers with this similar structure can be found in the literature as resonant regulator [37], PIS compensator [38], stationary-frame generalized integrator [39], etc. The details following an adaptive approach which yields a similar structure con be found in [48].

5.4.2 Regulation loop

To solve the regulation and the balance objectives, it is assumed that the current tracking objective has been reached (decoupling assumption), that is, $\mathbf{i}_{S\alpha\beta} = \mathbf{i}^*_{S\alpha\beta}$. Direct substitution of this in (5.21)-(5.23) and doing some straightforward computations yields the following

expressions

$$C\dot{x}_1 = g_1\mathbf{v}_{S\alpha\beta}^2 - \frac{2x_1}{R} + \varphi_1 \tag{5.30}$$

$$C\dot{x}_2 = g_2\mathbf{v}_{S\alpha\beta}^2 - \frac{2x_2}{R} + \varphi_2 \tag{5.31}$$

$$C\dot{x}_3 = g_3\mathbf{v}_{S\alpha\beta}^2 - \frac{2x_3}{R} + \varphi_3 \tag{5.32}$$

where φ_1, φ_2 and φ_3 are signals considered as disturbances, which are composed mainly by higher order harmonics, and , and $\mathbf{v}_{S\alpha\beta}^2 = v_{S\alpha}^2 + v_{S\beta}^2$. This can be easily realized by observing that the symmetric matrices $\mathbf{M}_1$, $\mathbf{M}_2$ and $\mathbf{M}_3$ have the following properties.

$$\mathbf{M}_1^2 = \mathbf{M}_2^2 = \mathbf{M}_3^2 = \boldsymbol{\mathcal{I}}_2 \quad \text{[involution]}$$

$$\mathbf{M}_2\mathbf{M}_3 = (\mathbf{M}_3\mathbf{M}_2)^\top$$

$$\boldsymbol{\xi}_{\alpha\beta}^\top\mathbf{M}_2\mathbf{M}_3\boldsymbol{\xi}_{\alpha\beta} = \boldsymbol{\mathcal{O}}_2 \ , \ \forall\boldsymbol{\xi}_{\alpha\beta} \ \text{[skew-simmetry]}$$

$$\boldsymbol{\xi}_{\alpha\beta}^\top\mathbf{M}_2\boldsymbol{\xi}_{\alpha\beta} = \xi_\alpha^2 - \xi_\beta^2$$

$$\boldsymbol{\xi}_{\alpha\beta}^\top\mathbf{M}_3\boldsymbol{\xi}_{\alpha\beta} = 2\xi_\alpha\xi_\beta$$

where $\boldsymbol{\mathcal{I}}_2$ is the identity matrix and $\boldsymbol{\mathcal{O}}_2$ is the zero matrix, both of dimension 2×2. Moreover, if vector $\mathbf{x}_{\alpha\beta}$ is purely sinusoidal, then the last two products yields only second harmonics.

The regulation objective is solved by designing g_1, g_2 and g_3 which are required to construct $\mathbf{i}_{S\alpha\beta}^*$. This control loop is formed by a proportional plus integral (PI) scheme operating on the corresponding error signal $\tilde{x}_1$, $\tilde{x}_2$ and $\tilde{x}_3$ as follows

$$g_1\mathbf{v}_{S,RMS}^2 = -k_{p1}\tilde{x}_1 - k_{i1}\int_0^t \tilde{x}_1 dt$$

$$g_2\mathbf{v}_{S,RMS}^2 = -k_{p2}\tilde{x}_2 - k_{i2}\int_0^t \tilde{x}_2 dt$$

$$g_3\mathbf{v}_{S,RMS}^2 = -k_{p3}\tilde{x}_3 - k_{i3}\int_0^t \tilde{x}_3 dt$$

where k_{p1}, k_{i1}, k_{p2}, k_{i2}, k_{p3} and k_{i3} are the proportional and integral gains, and $v_{S,RMS}$ is the RMS value of the source voltages vector, which is considered a constant.

5.4.3 Voltage balance loop

As in the regulation loop, it is also assumed here that $\mathbf{i}_{S\alpha\beta} = \mathbf{i}_{S\alpha\beta}^*$, or equivalently, $\mathbf{i}_{S123} = \mathbf{i}_{S123}^*$. Moreover, it is assumed that the regulation loop has been tuned in such a way that g_1, g_2 and g_3 reach the equilibrium much faster than the balance loop. Additionally, the influence of g_2 and g_3 can be neglected from subsystem (5.24)-(5.26) as they are considerably

smaller than g_1. Thus, after some straightforward computations, the expressions (5.24)-(5.26) can be rewritten as

$$C\dot{y}_1 = \delta_1(g_1 v_{S1} - i_{01}) - \frac{2y_1}{R} \tag{5.33}$$

$$C\dot{y}_2 = \delta_2(g_1 v_{S2} - i_{02}) - \frac{2y_2}{R} \tag{5.34}$$

$$C\dot{y}_3 = \delta_3(g_1 v_{S3} - i_{03}) - \frac{2y_3}{R} \tag{5.35}$$

For the voltage balance objective, the control inputs δ_1, δ_2 and δ_3 are designed to force the difference of the squares of the capacitor voltages to zero. It is proposed to build this control loop as follows

$$\delta_1 = \rho_1 v_{S1} \ , \ \delta_2 = \rho_2 v_{S2} \ , \ \delta_3 = \rho_3 v_{S3}$$

where the auxiliary variables ρ_1, ρ_2 and ρ_3 are formed by PI schemes over the corresponding y_1, y_2 and y_3 as follows

$$\rho_1 = -\beta_{p1} y_1 - \beta_{i1} \int_0^t y_1 dt$$

$$\rho_2 = -\beta_{p2} y_1 - \beta_{i2} \int_0^t y_2 dt$$

$$\rho_3 = -\beta_{p3} y_3 - \beta_{i3} \int_0^t y_3 dt$$

where β_{p1}, β_{p2}, β_{p3}, β_{i1}, β_{i2} and β_{i3} are the proportional and integral gains. It is proposed to computed the input control δ_1, δ_2 and δ_3 as where

$$\begin{bmatrix} i^*_{S1} \\ i^*_{S2} \\ i^*_{S3} \end{bmatrix} = A \begin{bmatrix} i^*_{S\alpha} \\ i^*_{S\beta} \end{bmatrix} = A i^*_{S\alpha\beta}$$

It is important to remark that, for a proper functioning of the above balance compensator, the voltage regulation loop should be tuned in such a way that the dynamics of subsystem (5.21)-(5.23), are faster than the dynamics of subsystem (5.24)-(5.26). I other words, the regulation task should be faster than the balance task. This allows to consider that g_1, g_2 and g_3 have practically reached their corresponding values before the balance has been accomplished. In fact, g_2 and g_3 are much smaller compared to g_1.

Figure 5.2 depicts a detailed block diagram of the completed proposed controller.

Figure 5.3 depicts how the control signals are combined in order to obtain the duty ratios.

5.4.4 Design criteria for the controller parameters

The bandwidth of the controller frequency response is limited by the maximum frequency of sampling/commutation. Usually, the bandwidth of the current loop is desired to be 1/10 of the sampling frequency. Based on this, an approximate procedure is followed to find an initial setting of the parameters for the current tracking control loop. First, it is proposed

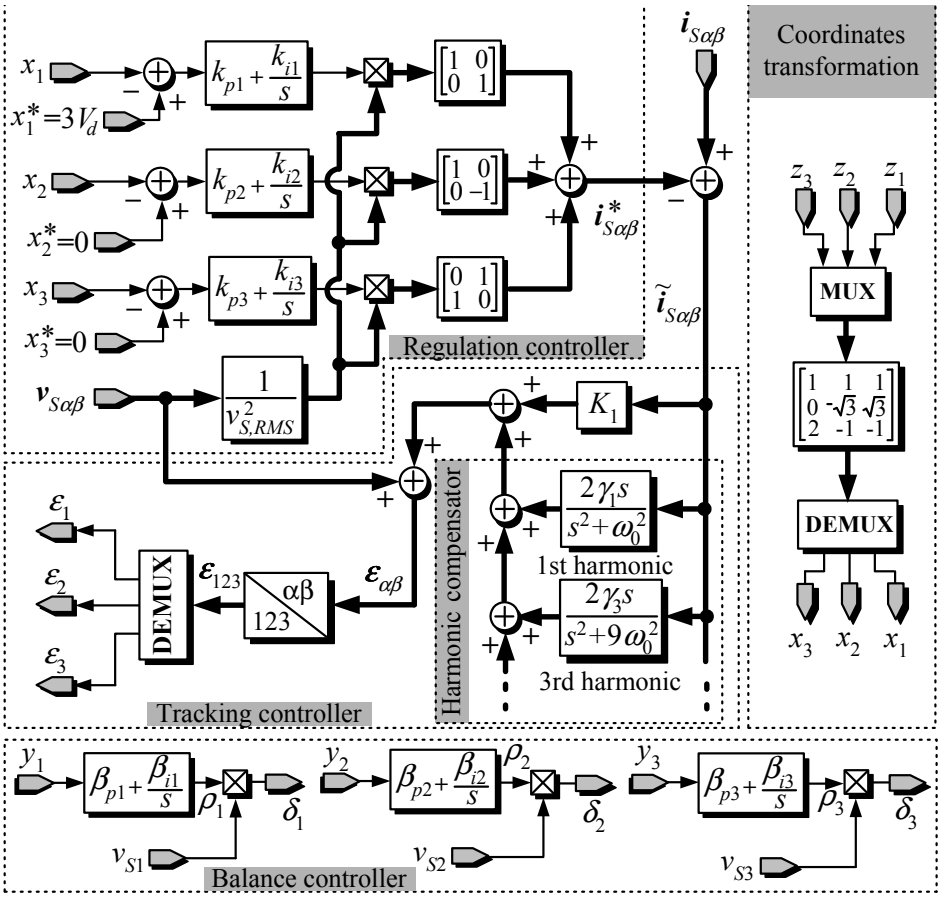

Figure 5.2: Block diagram of the overall controller including tracking, regulation and balance control loops.

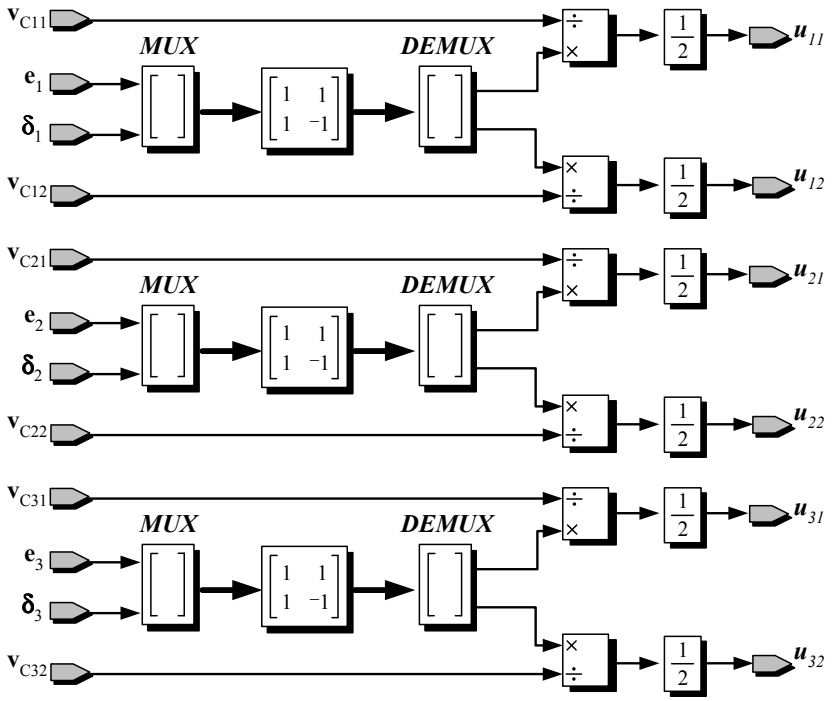

Figure 5.3: Block diagrams of the controls combinations to generate the control inputs in the original coordinates.

to set K_1 equal to $2\pi f_{ic}L$, where f_{ic} is the desired current loop bandwidth, in this case, $f_{ic} = f_{sw}/10$. Second, the remaining transfer function seen by the plurality of resonant filters is a first order low pass filter having a pole at $2\pi f_{ic}$. Disregarding, for simplicity, the influence of such a pole, the gain γ_k can be set as $\gamma_k = T_{k\gamma}$, where $T_{k\gamma}$ is the desired response time for each harmonic component (evaluated between the 10% and 90% of a step response of the amplitude of the corresponding sinusoidal perturbation). This relation is exact only when different band-pass filters give independent contributions. In a general case, however, this procedure gives a useful estimate of controller parameters given the desired response time for various harmonic components.

In the first outer loop, corresponding to the regulation of the capacitor voltages, the parameter selection is guided by conventional techniques given the desired regulation loop bandwidth and phase margin. Note, however, that due to the ripple on the DC voltage at twice the supply frequency during unbalanced conditions, the voltage loop bandwidth should be limited to approximately 10-20 Hz in order to avoid possible amplification of the second harmonic in the line current reference.

In the second outer loop, corresponding to the balance of the capacitor voltages, the parameter selection is guided also by conventional techniques. The main consideration in this outer loop is that the response in frequency of the controllers is limited by the response in frequency of the first outer loop. The response in frequency in this loop is usually set 1/5 of the response in frequency of the regulation loop.

5.5 Numerical results

Simulations using PSCAD 4.0 have been carried out. A three phase voltage source of 220V_{rms}, f_0=60Hz (ω_0=377rad/s) has been considered. A three-phase diode bridge rectifier with a resistive load taking values of 20Ω and 100Ω is considered as the nonlinear load. To create the unbalance, a resistor of 100Ω is connected between two phases. This load produces an unbalanced distorted current containing odd harmonics of the fundamental frequency (60Hz). The active filter has been designed with parameters $L = 3\text{mH}$, $C = 2200\,\mu\text{F}$, $R = 2.2\ \text{k}\Omega$. The switching frequency for the switching devices is fixed to 20kHz.

Figure 5.4 shows that the compensated source current $i_{S1}(t)$ (second plot) is an almost sinusoidal signal in phase with the source voltage v_{S1} (top plot), despite of the highly distorted load current i_{01} (third plot). In the bottom plot the injected current i_1 is presented. Figure 5.5 shows the capacitors voltages transient response (on each plot the two voltages on the same branch are presented) when the load in the diode bridge rectifier is changed from 100 Ω to 20 Ω and back to 100Ω. It is shown that after a relatively small transient, all capacitor voltages converges towards their common reference 150V_{DC}.

Figure 5.6 shows the scaled apparent conductance $g_1 v_{S,RMS}^2$ and extra control inputs $g_2 v_{S,RMS}^2$ and $g_3 v_{S,RMS}^2$ during the same transient. Notice that, $g_1 v_{S,RMS}^2$ reaches a constant value proportional to the total dissipated power, while $g_2 v_{S,RMS}^2$ and $g_3 v_{S,RMS}^2$ reach zero in average after a relatively short transient.

Finally, Fig.5.7 shows the injected voltage e_1 as computed in the control algorithm (in gray) and the resulting modulated signal using the multicarrier phase-shifted modulation algorithm.

5.6 Conclusions

In this chapter a model for the cascade H-bridge three-phase multilevel converter was proposed. A controller exploiting the structure of the system model was also proposed. It has been highlighted that while the current tracking and regulation problems could be solved in a quite familiar way, the balancing of the capacitor voltages required a more involved process. In fact, it was shown that this balancing was possible after the introduction of extra control inputs that basically distorted the current reference. This distortion was, however, present during transients only, and vanishes in the steady state. The effectiveness of the proposed controller open the possibility to apply a similar process to other topologies of multilevel converters that present the problem of balancing, and whenever the number of explicitly available control inputs is limited.

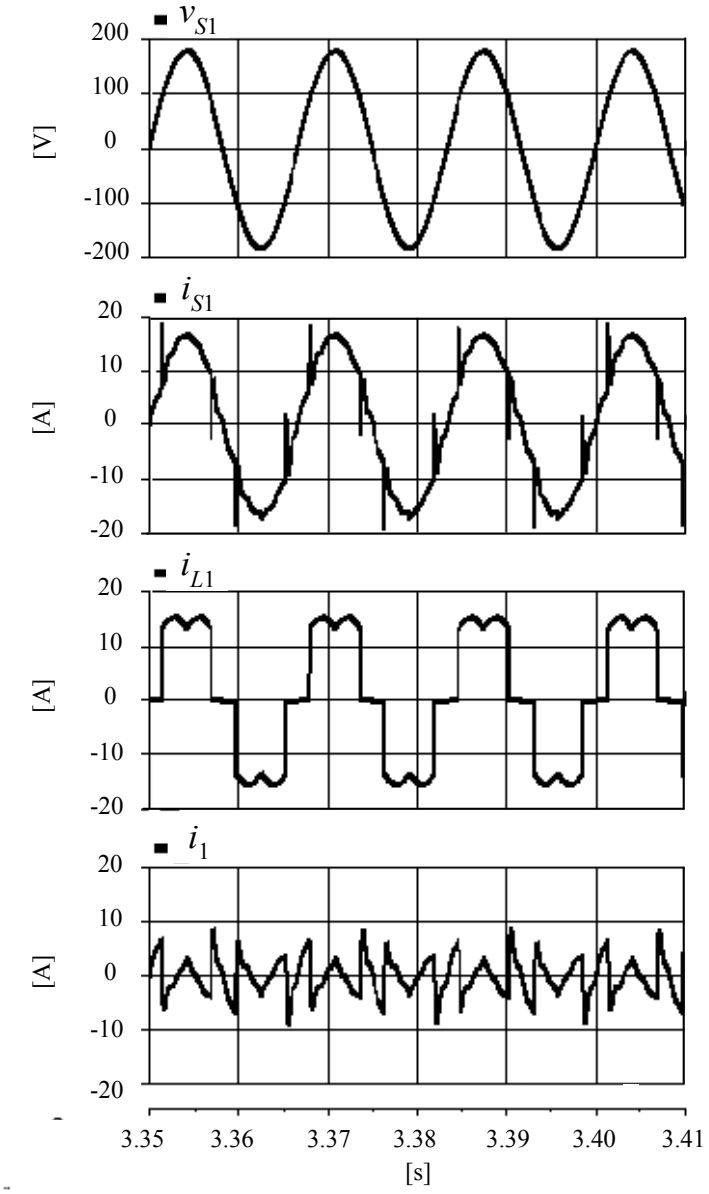

Figure 5.4: Steady state response with the proposed solution of **(from top to bottom)**: line voltage v_{S1}, line current i_{S1}, load current i_{01}, and injected current i_1.

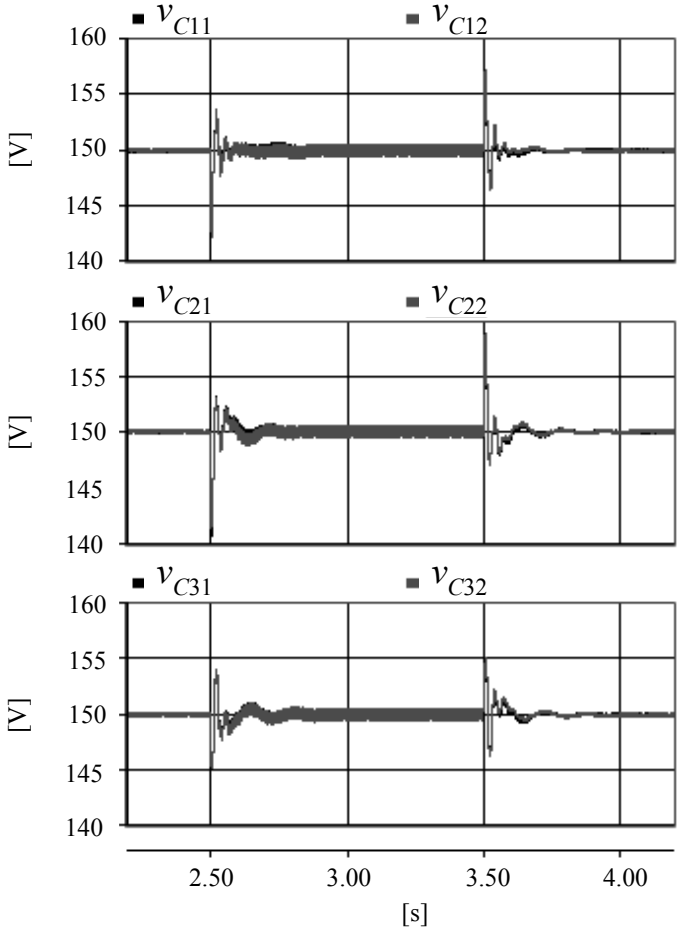

Figure 5.5: Transient response of the capacitors voltages during a load change.

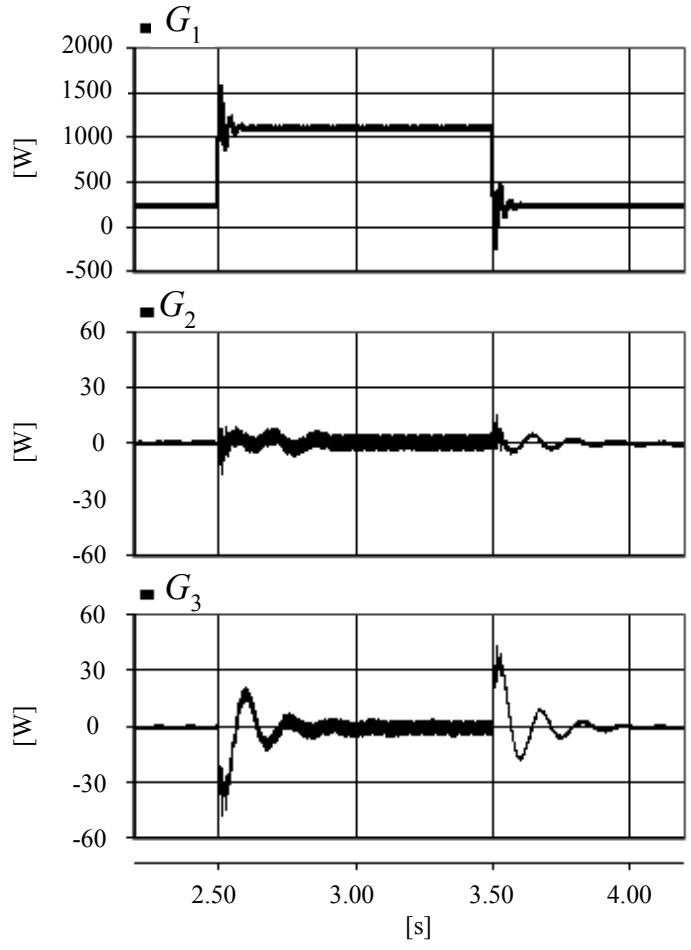

Figure 5.6: Transient response of **(from top to bottom)**: scaled apparent conductance $G_1 = g_1 v_{S,RMS}^2$ (dissipated power), and extra control inputs $G_2 = g_2 v_{S,RMS}^2$ and $G_3 = g_3 v_{S,RMS}^2$ during a load change.

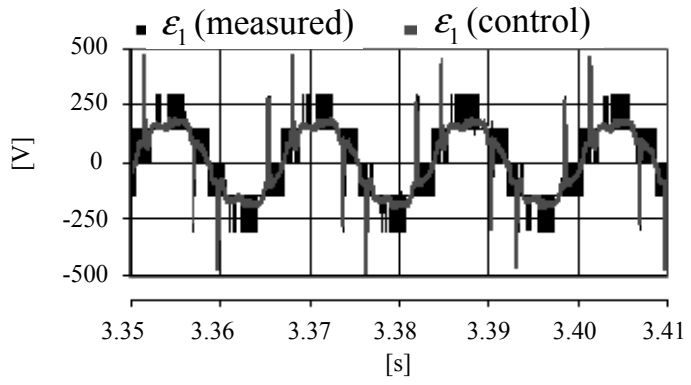

Figure 5.7: **(gray)** Injected voltage e_1 as computed in the control algorithm, and **(black)** the real injected voltage using a multicarrier phase-shifted modulation algorithm.

Chapter 6

A Phase-Locked-Loop based on an adaptive observer

6.1 Introduction

In general, a phase-locked loop (PLL) is a control system that generates an alternating signal, usually a sinusoidal signal, coming out of an oscillator, which is compared to a reference signal with the idea of locking both frequency and phase shift. Thus, the scheme must respond to both the frequency and the phase shift deviations between the generated and the input signal, and act in such a way that this deviations are minimized. Under this scheme, a clean version of the input reference is obtained with additional information, such as the frequency and or the phase angle. In the case of grid connected systems the detection of the phase, amplitude and frequency of the utility grid are critical information for the control of distributed generation and storage systems, flexible ac transmission systems (FACTS), power line conditioners, uninterruptible power supplies (UPS) [55], [56] and other grid-connected power conditioning equipments. The magnitude and angle of the source voltage is used for the synchronization of the converter output variables, power flux calculations, or for the transformation of state variables into rotating reference frames [57][59]. Regardless of the technique used in the system detection, the amplitude and the phase must be fast and accurately obtained, even if the utility voltage is distorted.

In a three-phase system, the utility-voltage information can be easily obtained using a utility-voltage vector, as the magnitude and angle of the voltage vector indicate the amplitude and angle of the utility voltage, respectively. However, for a single-phase system, the utility-voltage information is much more difficult to acquire. Conventionally, the frequency and phase angle of a single-phase voltage are obtained by detecting the zero-cross point. Yet, this method cannot provide the utility-voltage information instantaneously and is very sensitive to noise.

In this chapter a PLL scheme is presented which is aimed to estimate the angular frequency of the utility voltage as well as a cleaned version of the distorted input voltage. The proposed scheme delivers the estimates of both angular frequency ω and utility voltage v_S, and the time derivative of the voltage $\dot{v}_S$. These signals are useful in many applications.

The idea behind the design of the proposed PLL consists in:

(i) Propose a model that can accurately reproduce the utility voltage. For this purpose is

considered the model of the input signal as a harmonic oscillator in which it is assumed that only the parameter $v_S(t)$, as a time varying signal, is available.

(ii) Based on the proposed model, a state estimator is designed to reconstruct v_S and its time derivative. The state estimator is built as a copy of the model with additional damping.

(iii) As the estimator expression involves the angular frequency, then an adaptation law is proposed following the Lyapunov approach.

A prototype has been built and experimental results are presented to asses its performance.

6.2 Model of the single phase grid voltage

Consider that the generator or the model that generates the input signal is a harmonic oscillator of the following form

$$\begin{array}{rcl} \dot{v}_S & = & -\omega_0 \varphi \\ \dot{\varphi} & = & \omega_0 v_S \end{array} \tag{6.1}$$

where ω_0 represents the fundamental frequency, v_S is a time varying signal, and φ is an auxiliary signal which is in quadrature with respect to v_S.

It is convenient to define $\psi = \varphi/\omega_0$, out of which

$$\begin{array}{rcl} \dot{v_S} & = & {\omega_0}^2 \psi \\ \dot{\psi} & = & v_S \end{array} \tag{6.2}$$

Defining $\theta \triangleq {\omega_0}^2$, the model that describes the generator of signal v_S can be rewritten as

$$\begin{array}{rcl} \dot{v_S} & = & -\theta \psi \\ \dot{\psi} & = & v_S \end{array} \tag{6.3}$$

6.3 Description of the proposed PLL

Based on model (6.3), the objective consists in designing an estimator for state variables v_S and ψ, and an adaptive law to reconstruct parameter θ (the square of the fundamental frequency). Out of this adaptive estimator, a clean version of the grid voltage can be obtained as well as an estimate for the fundamental frequency.

6.3.1 The single phase grid voltage estimator

The proposed estimator consist in a copy of the system model (6.3) to which a damping term is added, that is,

$$\begin{array}{rcl} \dot{\hat{v}}_S & = & -\hat{\theta}\hat{\psi} + \lambda \tilde{v}_S \\ \dot{\hat{\psi}} & = & \hat{v}_S \end{array} \tag{6.4}$$

where it has been defined $\tilde{v}_S \triangleq v_S - \hat{v}_S$; $\hat{v}_S$ and $\hat{\psi}$ represent the estimates of v_S and ψ, respectively; $\hat{\theta}$ is the estimate of the parameter θ; and λ is a positive design parameter used to introduce the required damping.

6.3.2 Estimation of the fundamental frequency

Following a Lyapunov approach, an adaptive law is proposed to reconstruct $\hat{\theta}$ involved in (6.4). For this purpose the following quadratic storage function is proposed

$$V = \frac{\tilde{v}_S^2}{2} + \frac{\tilde{\psi}^2}{2} + \frac{\tilde{\theta}^2}{2\gamma} \tag{6.5}$$

where $\tilde{\psi} \triangleq \psi - \hat{\psi}$, $\tilde{\theta} \triangleq \theta - \hat{\theta}$, and $\gamma > 0$ is the adaptation gain.

Its time derivative along the trajectories of the error model is made negative semidefinite by proposing the adaptive law

$$\dot{\hat{\theta}} = -\gamma \tilde{v}_S \hat{\psi} \quad , \quad \hat{\omega}_0 = \sqrt{\hat{\theta}} \tag{6.6}$$

This yields

$$\dot{V} = -\lambda \tilde{v_S}^2 \tag{6.7}$$

The stability and convergence study of the proposed scheme can be completed using Barbalat's arguments, or using the properties of the signals as follows: from the proposed adaptive law, all error signals are bounded, i.e. $\tilde{v}_S \in L_\infty$, $\tilde{\psi} \in L_\infty$, $\tilde{\theta} \in L_\infty$, equivalently all estimates are bounded as well, i.e., $\hat{v}_S \in L_\infty$, $\hat{\psi} \in L_\infty$, $\hat{\theta} \in L_\infty$. This implies that the time derivative of the error is bounded as well, i.e., $\dot{\tilde{v}}_S \in L_\infty$ (or equivalently $\dot{\hat{v}}_S \in L_\infty$). As $\dot{\tilde{v}}_S$ is continuous and bounded, and based on the fact that $\tilde{v}_S \in L_2 \bigcap L_\infty$, then $\tilde{v}_S \to 0$ and $\dot{\tilde{v}} \to 0$ as $t \to \infty$. This implies, in their turn, that $\dot{\tilde{\psi}} \to 0$ and $\tilde{\theta} \to 0$ as $t \to \infty$ and thus $\tilde{\psi}$ and $\tilde{\theta}$ (or equivalently $\hat{\theta}$) go to constant values. Considering $\tilde{v}_S \equiv 0$, then from the error model, $\theta\tilde{\psi} = \tilde{\theta}\hat{\psi}$, however, $\tilde{\theta}\hat{\psi}$ is a time varying periodic signal, and thus the only point where $\tilde{\theta}\hat{\psi}$ is a constant is at $\tilde{\theta}\hat{\psi} = 0$, and $\theta\tilde{\psi} = 0$ as well, then $\tilde{\psi} = 0$ and $\hat{\psi} = \psi$, and if $\psi \neq 0$ then $\tilde{\theta} = 0$.

Summarizing, the proposed PLL consists of the estimator (6.4) plus the adaptive law (6.6). A block diagram of the proposed PLL algorithm is depicted in Fig.6.1.

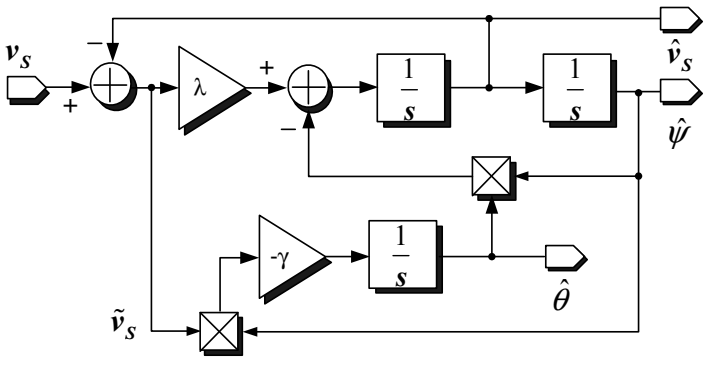

Figure 6.1: Block diagram of the proposed PLL algorithm.

6.4 Experimental results

For the experimental results, the proposed PLL algorithm was implemented using analog devices. The implementation involves Operational Amplifiers, multipliers and passive elements.

Figure 6.2 shows the transient response obtained with the proposed PLL algorithm during a start-up. Notice that, after a relatively short transient, both signals, the estimated voltage $\hat{v}_S$ and estimated $\hat{\theta}$, reach their desired values. Moreover, it is observed that the response for the estimated $\hat{\theta}$ (bottom) does not show overshoot.

Figure 6.3 shows the zoom of the transient response obtained with the proposed PLL algorithm. Notice that the estimated voltage $\hat{v}_S$ tracking the measured voltage v_S after a relatively short transient.

Figure 6.4 depicts the response of the proposed PLL when the utility frequency is changed in steps form 20 to 120 Hz. Notice that the estimated voltage $\hat{v}_S$ remains its amplitude at the desired constant value despite the changes in the frequency.

Figure 6.5 depicts the XY plot of estimated $\hat{v_S}$ versus estimated $\hat{\psi}$. Notice that the response of the proposed PLL correspond to a harmonic oscillator.

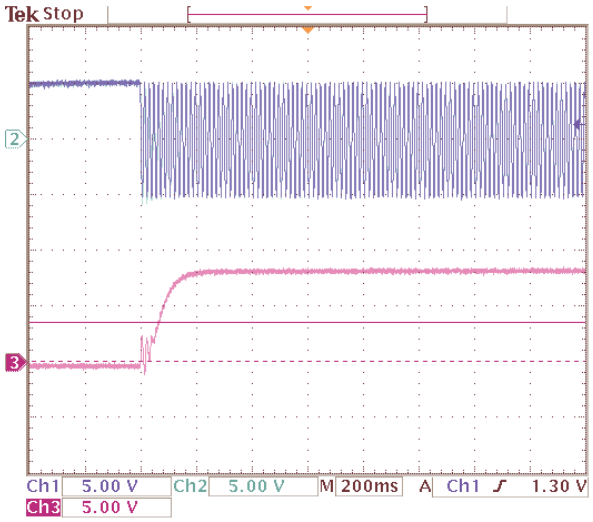

Figure 6.2: Response of the proposed PLL scheme **(top)** estimated $\hat{v}_S$ and **(bottom)** estimated $\hat{\theta}$.

6.5 Conclusions

In this chapter a PLL scheme was presented which was aimed to estimate the fundamental frequency, and both source voltage and its time derivative. The design process considered the model of the input signal as a harmonic oscillator in which it was assumed that only the signal $v_S(t)$ was available. Based on the proposed model, a state estimator was designed to reconstruct a copy of such input signal. The state estimator was built as a copy of the model

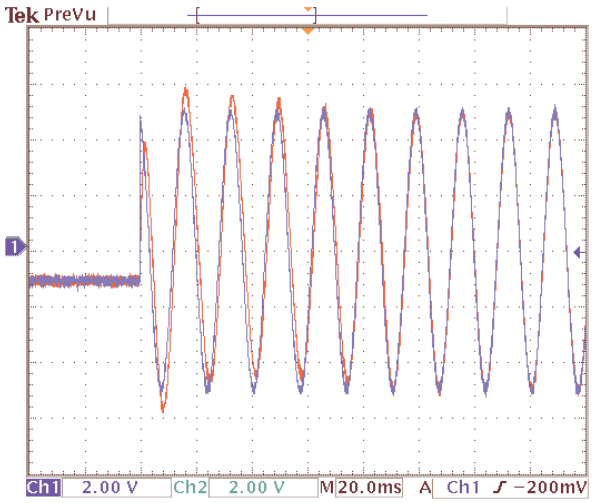

Figure 6.3: Zoom of the transient response of the estimated $\hat{v}_S$ and measured v_S.

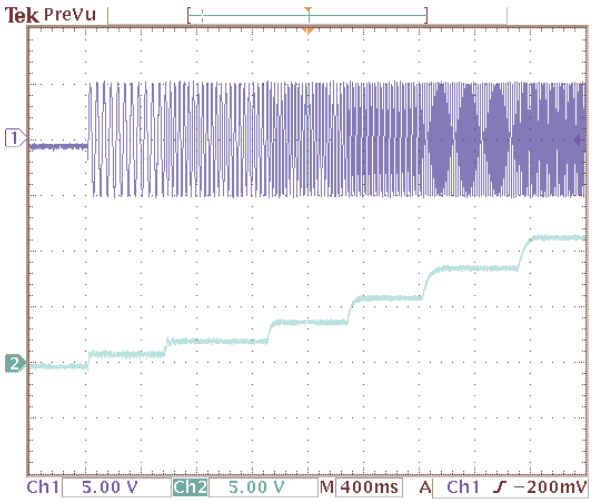

Figure 6.4: Response of the proposed PLL when the utility frequency is changed in steps from 20 to 120 Hz. **(top)** Utility voltage v_S,and **(bottom)** estimated θ.

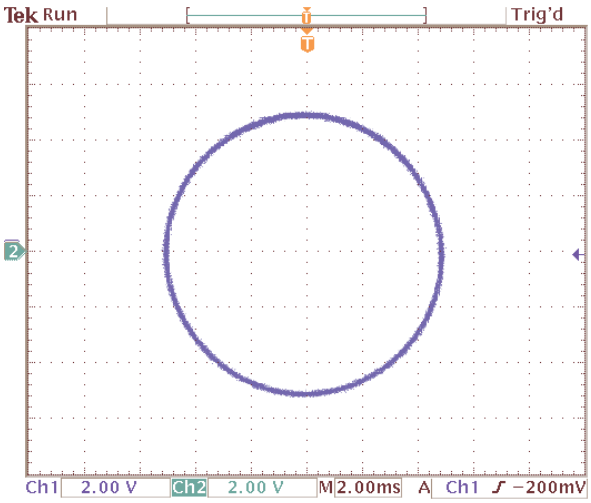

Figure 6.5: Depicts the XY plot of estimated $\hat{v_S}$ versus estimated $\hat{\psi}$.

with additional damping. An adaptation law was incorporated to reconstruct the angular frequency. It was shown that the proposed PLL scheme is robust to frequency changes.

Chapter 7

FRF-PLL

7.1 Introduction

One crucial aspect in the control of three-phase grid-connected power converters is the detection of the fundamental-frequency positive-sequence component of the utility voltage under unbalanced and distorted conditions. Specifically, the detection of the positive-sequence voltage component at fundamental frequency is essential for the control of distributed generation and storage systems, flexible ac transmission systems (FACTS), power line conditioners and uninterruptible power supplies (UPS) [55], [56] and others grid-connected power conditioning equipments. The magnitude and angle of the source voltage is used for the synchronization of the converter output variables, power flux calculations, or for the transformation of state variables into rotating reference frames [57][59]. Regardless of the technique used in the system detection, the amplitude and the phase must be fast and accurately obtained, even if the utility voltage is distorted.

The most extended technique used for frequency-insensitive positive-sequence detection is the conventional three-phase PLL based on the synchronous reference frame (SRF-PLL). In the conventional SRF-PLL, the three-phase voltage vector is translated from the natural reference frame to the rotating reference frame by using a combination of Clarke's and Park's transformations. The angular position of this reference frame is controlled by a feedback loop which regulates the q-component of the positive sequence of the voltage to zero. Therefore, in steady-state, the detected d-component depicts the voltage vector amplitude, while its phase angle is determined by the output of the feedback loop. Under ideal utility conditions, i.e., neither harmonic distortion nor unbalance are present, a high bandwidth feedback loop of the SRF-PLL yields a fast and precise detection of the phase angle and amplitude of the utility voltage vector. In the case that the utility voltage is distorted with high-order harmonics, the bandwidth of the SRF-PLL feedback loop can be reduced to reject and cancel out the effect of the harmonics on the output. However, the PLL bandwidth reduction is not an acceptable solution. The problem of estimating this fundamental component gets even more challenging in case of presence of unbalanced grid voltages.

The present chapter presents an algorithm to implement a phase-locked loop (PLL) which is able to provide an estimation of the angular frequency, and both the positive and negative sequences of the fundamental component of an unbalanced three-phase signal. These sequences are provided in fixed reference frame coordinates, and thus the proposed algorithm

is referred as fixed reference frame PLL (FRF-PLL). In fact, the FRF-PLL does not require transformation of variables into the synchronous reference frame coordinates as in most PLL schemes. The detection of the positive sequence component of the source voltage at fundamental frequency is essential for the control and synchronization of systems coupled with the electric network, which are required to run even under grid disturbances such as unbalanced voltages, voltages sags, harmonic distortion and angular frequency variations. The design of the FRF-PLL is based on a complete description of the source voltage involving both positive and negative sequences in stationary coordinates and considering that the angular frequency is uncertain. Therefore the FRF-PLL is intended to perform properly under unbalanced conditions, and to be robust against angular frequency variations, providing a fast and precise response. Although not considered in the design, it is shown that the scheme is also robust against harmonic distortion present in the source voltage signal.

The idea behind the design consists in:

(i) Propose a model that can accurately reproduce the evolution of an unbalanced three-phase signal. For this purpose both positive and negative sequence components of the three-phase signal are considered. Most PLLs reported in the literature consider the positive sequence only. In other words, they are all based on the model description of the three-phase line voltage signal $\dot{v}_{\alpha\beta} = J\omega v_{\alpha\beta}$, which holds for the balanced case only. In contrast, the present work introduces a new auxiliary variable $\varphi_{\alpha\beta}$, which permits to describe an unbalanced three-phase line voltage signal completely. To realize this, notice that the voltage signal can be represented as the sum of both sequences, i.e., $v_{\alpha\beta} = v^p_{\alpha\beta} + v^n_{\alpha\beta}$, and define the auxiliary variable as the difference between both sequences, i.e., $\varphi_{\alpha\beta} = v^p_{\alpha\beta} - v^n_{\alpha\beta}$. Out of this, the three-phase signal $v_{\alpha\beta}$ can be fully described by the system $\dot{v}_{\alpha\beta} = J\omega\varphi_{\alpha\beta}$, $\dot{\varphi}_{\alpha\beta} = J\omega v_{\alpha\beta}$.

(ii) Based on the proposed model, a state estimator is designed to reconstruct both positive and negative sequences of the three-phase signal. The state estimator is built as a copy of the model with additional damping.

(iii)As the estimator expression involves the angular frequency, then an adaptation law is incorporated to reconstruct the angular frequency as well.

The stability and convergence study of the proposed FRF-PLL scheme follow the Lyapunov's approach, without involving any linearization process.

7.2 Model of the grid voltage in unbalanced condition

In what follows, it is considered that the three-phase voltage signal, originally in three-phase coordinates $v_{123} = [v_1,\, v_2,\, v_3]^\top$, has been transformed to (fixed frame) $\alpha\beta$-coordinates using the following Clarke's transformation.

$$\mathbf{v}_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

This non-normalized Clarke's transformation could be preferred since $v_\alpha = v_1$, thus preserving the amplitude and phase angle of v_α equal to those of v_1. However, the algorithm

is not restricted to this transformation, and thus the normalized transformation could be used as well without further changes in the scheme.

Assume that, the source voltage signal is composed only by a fundamental component, and as the unbalanced operation case is considered, then the three-phase signal is described as the sum of its positive and negative sequences as follows

$$\mathbf{v}_{\alpha\beta} = \mathbf{v}^p_{\alpha\beta} + \mathbf{v}^n_{\alpha\beta} = \mathbf{e}^{\mathbf{J}\theta}\mathbf{V}^p_{dq} + \mathbf{e}^{-\mathbf{J}\theta}\mathbf{V}^n_{dq} \tag{7.1}$$

$$\mathbf{e}^{\mathbf{J}\theta} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}, \quad \mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{7.2}$$

where $\mathbf{V}^p_{dq} = \left[V^p_d, V^p_q\right]^\top$ and $\mathbf{V}^n_{dq} = \left[V^n_d, V^n_q\right]^\top$ are the vectors of coefficients, also referred as phasors, of the positive and negative sequences, respectively, of the fundamental component of $\mathbf{v}_{\alpha\beta}$.

Based on description (7.1), the following relationship is obtained

$$\begin{aligned} \dot{\mathbf{v}}_{\alpha\beta} &= \mathbf{J}\omega\mathbf{e}^{\mathbf{J}\theta}\mathbf{V}^p_{dq} - \mathbf{J}\omega\mathbf{e}^{-\mathbf{J}\theta}\mathbf{V}^n_{dq} \\ &= \mathbf{J}\omega\left(\mathbf{v}^p_{\alpha\beta} - \mathbf{v}^n_{\alpha\beta}\right) \end{aligned} \tag{7.3}$$

where ω represents the true angular frequency, and it has been used the fact that $\dot{\theta} = \omega$. It is also convenient to define $\boldsymbol{\varphi}_{\alpha\beta} \triangleq \mathbf{v}^p_{\alpha\beta} - \mathbf{v}^n_{\alpha\beta}$, out of which $\dot{\mathbf{v}}_{\alpha\beta} = \mathbf{J}\omega\boldsymbol{\varphi}_{\alpha\beta}$. Notice also that $\dot{\boldsymbol{\varphi}}_{\alpha\beta} = \mathbf{J}\omega\mathbf{e}^{\mathbf{J}\theta}\mathbf{V}^p_{dq} + \mathbf{J}\omega\mathbf{e}^{\mathbf{J}\theta}\mathbf{V}^n_{dq} = \mathbf{J}\omega\left(\mathbf{v}^p_{\alpha\beta} + \mathbf{v}^n_{\alpha\beta}\right)$. Therefore, the model that completely describes the generator of signal $\mathbf{v}_{\alpha\beta}$ is given by

$$\begin{aligned} \dot{\mathbf{v}}_{\alpha\beta} &= \mathbf{J}\omega\boldsymbol{\varphi}_{\alpha\beta} \\ \dot{\boldsymbol{\varphi}}_{\alpha\beta} &= \mathbf{J}\omega\mathbf{v}_{\alpha\beta} \end{aligned} \tag{7.4}$$

It is important to remark that the introduction of the auxiliary variable $\boldsymbol{\varphi}_{\alpha\beta}$ allows a complete description of the generator system in the unbalanced case (7.4).

Remark 7.1 In the balanced case, this description is reduced to $\dot{\mathbf{v}}_{\alpha\beta} = \mathbf{J}\omega\mathbf{v}_{\alpha\beta}$, which is the most common expression found in the literature. □

In fact, based on definition (7.1) and the definiton of $\varphi_{\alpha\beta}$, is possible to establish the following relationship

$$\begin{bmatrix} v_{\alpha\beta} \\ \varphi_{\alpha\beta} \end{bmatrix} = \begin{bmatrix} I_2 & I_2 \\ I_2 & -I_2 \end{bmatrix} \begin{bmatrix} {v_{\alpha\beta}}^p \\ {v_{\alpha\beta}}^n \end{bmatrix} \tag{7.5}$$

where I_2 is the 2x2 identity matrix.

As observed in (7.4), parameter ω appears in both rows of the system. This situation may difficult the estimation of ω. To overcome this issue, it is proposed to concentrate this parameter in a single row using the transformation

$$\boldsymbol{\psi}_{\alpha\beta} = \boldsymbol{\varphi}_{\alpha\beta}/\omega \tag{7.6}$$

This yields the following model

$$\begin{aligned} \dot{\mathbf{v}}_{\alpha\beta} &= \mathbf{J}\sigma\boldsymbol{\psi}_{\alpha\beta} \\ \dot{\boldsymbol{\psi}}_{\alpha\beta} &= \mathbf{J}\mathbf{v}_{\alpha\beta} \end{aligned} \tag{7.7}$$

where it has been defined $\sigma \triangleq \omega^2$ as the new parameter.

7.3 Description of the proposed FRF-PLL

Based on model (7.7), the objective consists in designing an estimator for state variables $\mathbf{v}_{\alpha\beta}$ and $\boldsymbol{\psi}_{\alpha\beta}$, and an adaptive law to reconstruct parameter σ, out of which positive and negative sequences of the grid voltage can be obtained as well as the angular frequency ω.

7.3.1 The grid voltage estimator

Estimation of the state variables $\mathbf{v}_{\alpha\beta}$ and $\boldsymbol{\psi}_{\alpha\beta}$ allows to obtain the positive sequence component, this according to $\mathbf{v}^p_{\alpha\beta} = \frac{1}{2}(\mathbf{v}_{\alpha\beta} + \boldsymbol{\varphi}_{\alpha\beta})$ and using (7.6). The proposed estimator consist in a copy of the system model (7.7) to which a damping term is added, that is,

$$\begin{aligned} \dot{\hat{\mathbf{v}}}_{\alpha\beta} &= \mathbf{J}\hat{\sigma}\hat{\boldsymbol{\psi}}_{\alpha\beta} + \lambda\tilde{\mathbf{v}}_{\alpha\beta} \\ \dot{\hat{\boldsymbol{\psi}}}_{\alpha\beta} &= \mathbf{J}\hat{\mathbf{v}}_{\alpha\beta} \end{aligned} \tag{7.8}$$

where it has been defined $\tilde{\mathbf{v}}_{\alpha\beta} \triangleq \mathbf{v}_{\alpha\beta} - \hat{\mathbf{v}}_{\alpha\beta}$; $\hat{\mathbf{v}}_{\alpha\beta}$ and $\hat{\boldsymbol{\psi}}_{\alpha\beta}$ represent the estimates of $\mathbf{v}_{\alpha\beta}$ and $\boldsymbol{\psi}_{\alpha\beta}$, respectively; $\hat{\sigma}$ is the estimate of the parameter σ; and λ is a positive design parameter used to introduce the required damping.

7.3.2 Estimation of the angular frequency

Following a Lyapunov approach an adaptive law is proposed to reconstruct $\hat{\sigma}$ involved in (7.8). For this purpose the following quadratic storage function is proposed

$$W = \frac{\tilde{\mathbf{v}}^\top_{\alpha\beta}\tilde{\mathbf{v}}_{\alpha\beta}}{2} + \frac{\sigma\tilde{\boldsymbol{\psi}}^\top_{\alpha\beta}\tilde{\boldsymbol{\psi}}_{\alpha\beta}}{2} + \frac{\tilde{\sigma}^2}{2\gamma} \tag{7.9}$$

where $\tilde{\boldsymbol{\psi}}_{\alpha\beta} \triangleq \boldsymbol{\psi}_{\alpha\beta} - \hat{\boldsymbol{\psi}}_{\alpha\beta}$, $\tilde{\sigma} \triangleq \sigma - \hat{\sigma}$, and $\gamma > 0$ is the adaptation gain. Its time derivative along the trajectories of the error model is made negative semidefinite by proposing the adaptive law

$$\dot{\hat{\sigma}} = \gamma\tilde{\mathbf{v}}^\top_{\alpha\beta}\mathbf{J}\hat{\boldsymbol{\psi}}_{\alpha\beta} \quad , \quad \hat{\omega} = \sqrt{\hat{\sigma}} \tag{7.10}$$

This yields

$$\dot{W} = -\lambda\tilde{\mathbf{v}}^\top_{\alpha\beta}\tilde{\mathbf{v}}_{\alpha\beta} \tag{7.11}$$

The stability and convergence study of the proposed scheme can be completed using Lasalle's arguments, or using the properties of the signals as follows. From the proposed adaptive law, all error signals are bounded, i.e. $\tilde{v}_{\alpha\beta} \in L_\infty$, $\tilde{\psi}_{\alpha\beta} \in L_\infty$, $\tilde{\sigma}_{\alpha\beta} \in L_\infty$, equivalently all estimates are bounded as well, i.e., $\hat{v}_{\alpha\beta} \in L_\infty$, $\hat{\psi}_{\alpha\beta} \in L_\infty$, $\hat{\sigma}_{\alpha\beta} \in L_\infty$. This implies that the time derivative of the error is bounded as well, i.e., $\dot{\tilde{v}}_{\alpha\beta} \in L_\infty$ (or equivalently $\dot{\hat{v}}_{\alpha\beta} \in L_\infty$). As $\dot{\tilde{v}}_{\alpha\beta}$ is continuous and bounded, and based on the fact that $\tilde{v}_{\alpha\beta} \in L_2 \bigcap L_\infty$, then $\tilde{v}_{\alpha\beta} \to 0$ and $\dot{\tilde{v}}_{\alpha\beta} \to 0$ as $t \to \infty$. This implies, in their turn, that $\dot{\tilde{\psi}}_{\alpha\beta} \to 0$ and $\tilde{\sigma} \to 0$ as $t \to \infty$ and thus $\tilde{\psi}_{\alpha\beta}$ and $\tilde{\sigma}$ (or equivalently $\hat{\sigma}$) go to constant values. Considering $\tilde{v}_{\alpha\beta} \equiv 0$, then from the error model, $\sigma\tilde{\psi}_{\alpha\beta} = \tilde{\sigma}\hat{\psi}_{\alpha\beta}$, however, $\tilde{\sigma}\hat{\psi}_{\alpha\beta}$ is a rotating vector while simultaneously the product $\sigma\tilde{\psi}_{\alpha\beta}$ is a constant, hence, the only possibility is that $\tilde{\sigma} \to 0$ and

$\tilde{\psi}_{\alpha\beta} \rightarrow 0$ as well. As no linearization process has been involved at all, both stability and convergence might be stated globally. This is however, not fully true, as the operative region is bounded due to physical construction limitations.

7.3.3 Estimation of positive and negative sequences of the grid voltage

Out of estimator (7.8) and adaptation (7.10), the positive and negative sequences of the grid voltage can now be reconstructed as follows

$$\begin{aligned} \hat{\mathbf{v}}^{p}_{\alpha\beta} &= \frac{1}{2}(\hat{\mathbf{v}}_{\alpha\beta} + \hat{\omega}\hat{\boldsymbol{\psi}}_{\alpha\beta}) \\ \hat{\mathbf{v}}^{n}_{\alpha\beta} &= \frac{1}{2}(\hat{\mathbf{v}}_{\alpha\beta} - \hat{\omega}\hat{\boldsymbol{\psi}}_{\alpha\beta}) \end{aligned} \tag{7.12}$$

Summarizing, the proposed FRF-PLL consists of the estimator (7.8) and adaptive law (7.10), where both positive and negative sequence are computed according to (7.12).

A block diagram of the proposed FRF-PLL algorithm is depicted in Fig.7.2. The proposed FRF-PLL is connected to the grid according to Fig.7.1.

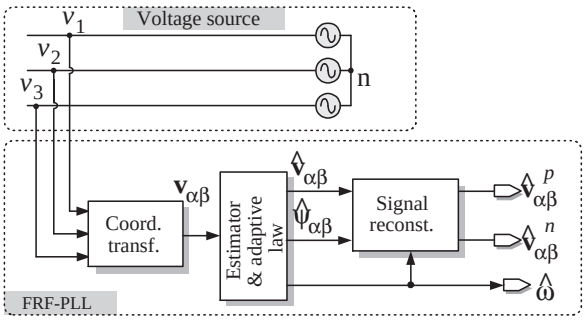

Figure 7.1: Connection of the proposed FRF-PLL to the electric utility.

7.4 Tuning of the FRF-PLL algorithm

For a first approximation of tuning of parameters λ and γ consider that the system is in balanced operation, that is, $\boldsymbol{\psi}_{\alpha\beta} \cong \mathbf{v}_{\alpha\beta}$, out of which, $\boldsymbol{\varphi}_{\alpha\beta} \cong \boldsymbol{\psi}_{\alpha\beta}/\omega$, and thus it can also be assumed that $\hat{\boldsymbol{\varphi}}_{\alpha\beta} \cong \hat{\boldsymbol{\psi}}_{\alpha\beta}/\omega$. Moreover, consider that $\hat{\psi} \cong \omega\hat{\omega}$. This yields the following system

$$\dot{\hat{\mathbf{v}}}_{\alpha\beta} = \mathbf{J}\hat{\omega}\hat{\mathbf{v}}_{\alpha\beta} + \lambda\hat{\mathbf{v}}_{\alpha\beta} \tag{7.13}$$

$$\dot{\hat{\omega}} = \frac{\gamma}{\omega^2}\mathbf{v}^{\top}_{\alpha\beta}\mathbf{J}\hat{\mathbf{v}}_{\alpha\beta} \tag{7.14}$$

which represents, in fact, the balanced version of the proposed estimator.

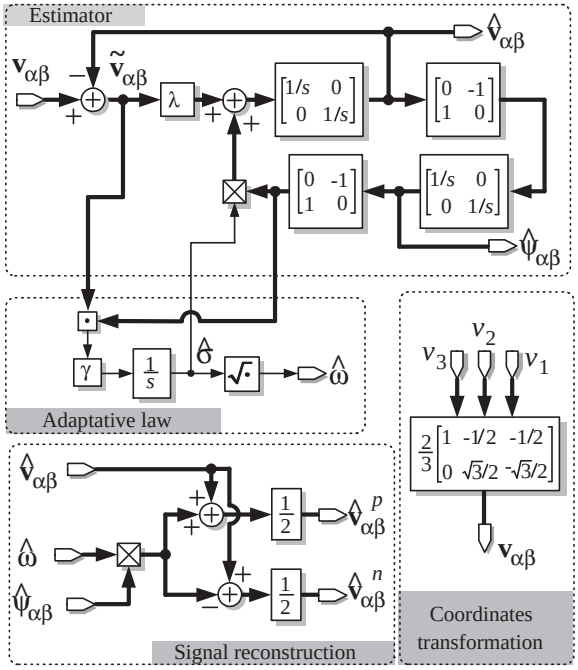

Figure 7.2: Block diagram of the proposed FRF-PLL algorithm.

Then, consider the coordinate transformation $x_1 = \mathbf{v}_{\alpha\beta}^{\top}\mathbf{J}\hat{\mathbf{v}}_{\alpha\beta}$, $x_2 = \mathbf{v}_{\alpha\beta}^{\top}\hat{\mathbf{v}}_{\alpha\beta}$ and $x_3 = \omega - \hat{\omega}$, which yields the system

$$\dot{x}_1 = -x_3 x_2 - \lambda x_1 \tag{7.15}$$
$$\dot{x}_2 = x_3 x_1 - \lambda x_2 + \lambda|\mathbf{v}_{\alpha\beta}|^2 \tag{7.16}$$
$$\dot{x}_3 = \frac{\gamma}{\omega^2} x_1 \tag{7.17}$$

where $|\mathbf{v}_{\alpha\beta}|$ is a constant representing the amplitude of the source voltage signal.

Linearization of system (7.15)-(7.17) around the equilibrium point $[\overline{x}_1, \overline{x}_2, \overline{x}_3,] = [0, |\mathbf{v}_{\alpha\beta}|^2, 0]$ yields the following LTI system

$$\dot{x}_1 = -|\mathbf{v}_{\alpha\beta}|^2 x_3 - \lambda x_1 \tag{7.18}$$
$$\dot{\tilde{x}}_2 = -\lambda \tilde{x}_2 \tag{7.19}$$
$$\dot{x}_3 = \frac{\gamma}{\omega^2} x_1 \tag{7.20}$$

Notice that (7.19) is a stable first order subsystem decoupled from a second order system composed by (7.18) and (7.20). Thus, a first approximation for the tuning of parameters λ and γ is based on the desired bandwidth frequency ω_{BW} of the frequency response of such a second order system. To facilitate the design, a damping ratio of $1/\sqrt{2}$ is considered, out of which the bandwidth equals the natural oscillation frequency of the second order system. As the algorithm involves the computation of projections between vectors of sinusoidal signals producing mainly a second order harmonic, then the bandwidth of the algorithm should be smaller than $2\omega_0$, where ω_0 is the nominal value of the angular frequency of the source voltage. It is common in practice to select the bandwidth between 1/2 to 1/10 of such frequency,

that is, $\omega_0/5 \lesssim \omega_{BW} \lesssim \omega_0/2$. Based on this consideration, the parameters can be tuned according to the following expressions

$$\begin{aligned} \lambda &\cong \sqrt{2}\omega_{BW} \\ \gamma &\cong \left(\frac{\omega_0 \omega_{BW}}{|\mathbf{v}_{\alpha\beta}|}\right)^2 \end{aligned} \tag{7.21}$$

7.5 Numerical results

In the numerical results the following parameters have been selected $\lambda = 300$ and $\lambda = 2.2\text{x}10^5$, which correspond approximately to a bandwidth of 24Hz (ω_{BW}=150 rad/s), considering a nominal frequency of 50Hz (ω_0=314.16 rad/s). For the numerical results the following cases have been considered for the utility voltage source:

(i) Balanced condition. The voltage source is formed only by a positive sequence of 100 V of amplitude and angular frequency of 50 Hz (314.16 rad/s), with a zero phase shift.

(ii) Unbalanced condition. The voltage source includes both a positive and a negative sequence components. The positive sequence has 100 V of amplitude at 50Hz (314.16 rad/s) and zero phase shift. For the negative sequence an amplitude of 30 V and zero phase shift are considered.

(iii) Utility frequency changes. Harmonics 3rd and 5th are added to the previous unbalanced signal to create a periodic distortion. Both harmonics have also a negative sequence to allow unbalance. Both the positive and the negative sequence have 10 V of amplitude and zero phase shift.

Figure 7.3 shows the transient response obtained with the proposed FRF-PLL algorithm when the utility voltage goes from a balanced to an unbalanced operation condition at time $t = 3$s. Notice that, after a relatively short transient, all signals return to their desired values. For instance, it is observed that the estimated phase angle (solid line) follows perfectly well the true phase angle (dashed line) after an almost imperceptible transient. The estimated frequency (solid line) is also maintained in its reference fixed to 316.14rad/s (dotted line) after a small transient. Moreover, the estimated positive-sequence voltages have an almost imperceptible variation.

Figure 7.4 presents the transient response of the proposed FRF-PLL to an unbalanced and distorted utility voltage and during a start-up operation. It is shown that after a relatively small transient the estimated phase angle (solid line) is synchronized to the true phase angle (dashed line). Similarly, the estimated angular frequency reaches, after a small transient, its reference (dotted line), which has been fixed to 316.14rad/s. The bottom plot shows that the estimated positive-sequence voltages reach their final amplitude of 100 V after a few cycles.

Figure 7.5 shows the transient response of the proposed FRF-PLL to a step change in the angular frequency of the source voltage going from 50Hz to 35Hz. It is shown that after a short transient the estimated phase angle follows perfectly well the true phase angle. It is shown that the estimated angular frequency, starting at a reference of 314.16rad/s, reaches its new reference fixed to 219.9rad/s in a relatively short time. The bottom plot shows that the estimated positive-sequence voltages maintain their amplitude after an almost imperceptible transient.

Figure 7.6 depicts the transient response of the proposed FRF-PLL to a step change in the angular frequency of the source voltage going from 35Hz to 50Hz. As in Fig. 7.5, the estimated phase angle follows perfectly well the true phase angle after a short transient. It is shown that the estimated angular frequency, starting at a reference of 219.9rad/s, reaches its new reference fixed to 314.16rad/s in a relatively short time. The bottom plot shows that the estimated positive-sequence voltages maintain their amplitude after an almost imperceptible transient.

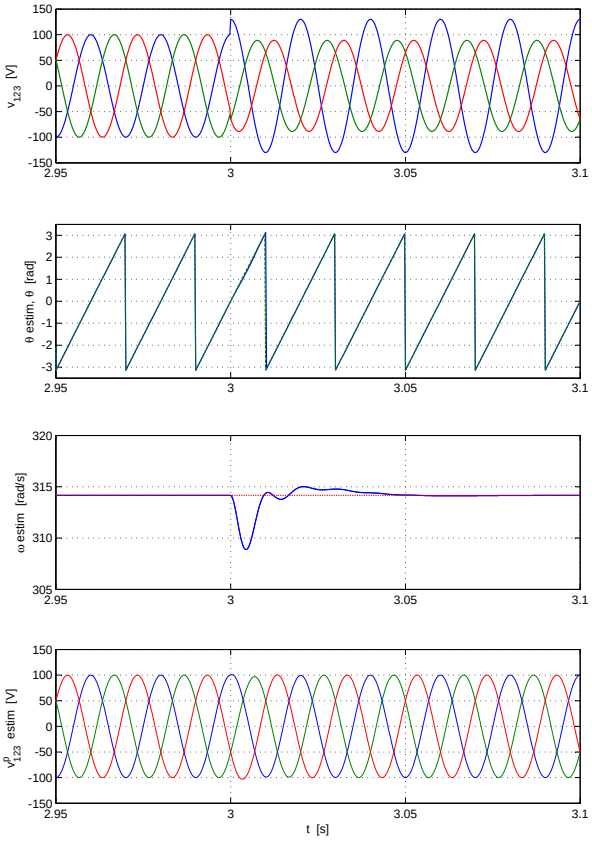

Figure 7.3: Depicts the transient response of the proposed FRF-PLL when the utility voltage goes from a balanced to an unbalanced condition. (from top to bottom) Utility voltage v_{123}, estimated phase angle $\hat{\theta}$, estimated angular frequency $\hat{\omega}$, and estimated positive-sequence voltage in the synchronous reference frame $\hat{v_{123}}^{p}$.

7.6 Experimental results

For the experimental results, the proposed FRF-PLL algorithm was programmed in a fixed-point DSP TMS320LF2407A. The following parameters have been selected: a bandwidth of 24 Hz ($\omega_{BW} = 150$ rad/s), considering a nominal frequency of 50 Hz ($\omega_0 = 314.16$ rad/s). It is considered that the input signals, are in (fixed frame) $\alpha\beta$-coordinates.

The following conditions have been considered for the utility voltage source:

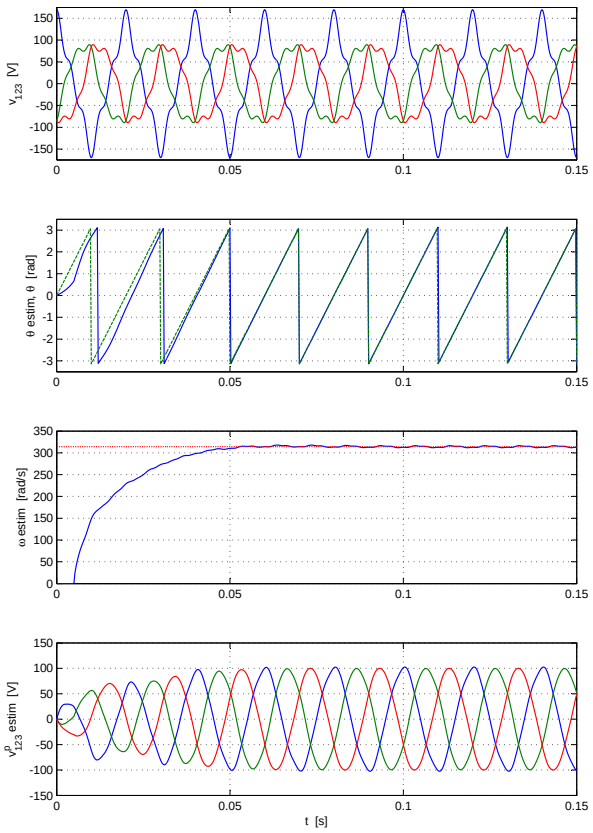

Figure 7.4: Depicts the response of the proposed FRF-PLL to an unbalanced distorted utility voltage during start-up. (from top to bottom) Utility voltage v_{123}, estimated phase angle $\hat{\theta}$, estimated angular frequency $\hat{\omega}$, and estimated positive-sequence voltage in the synchronous reference frame $\hat{v_{123}}^{p}$.

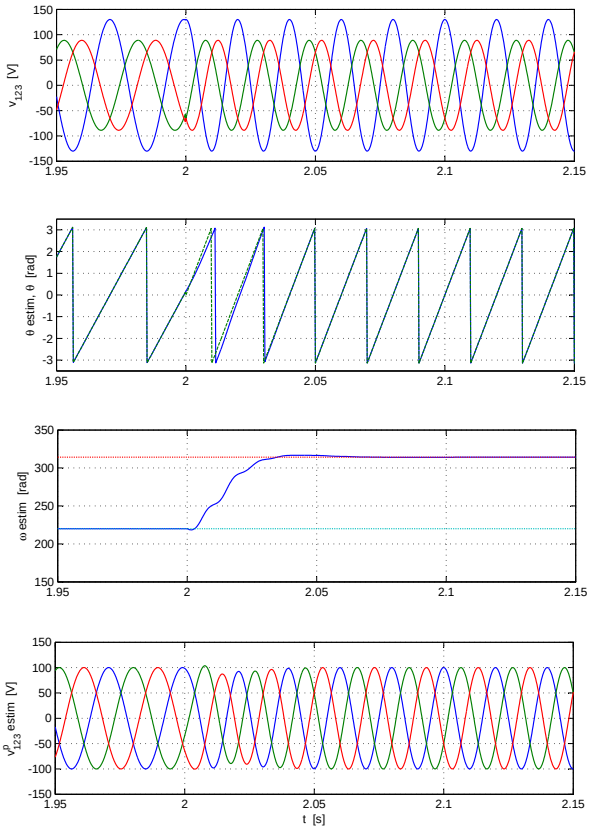

Figure 7.5: Depicts the transient response of the proposed FRF-PLL to a utility frequency change from 50 Hz to 35 Hz. (from top to bottom) Utility voltage v_{123}, estimated phase angle $\hat{\theta}$, estimated angular frequency $\hat{\omega}$, and estimated positive-sequence voltage in the synchronous reference frame $\hat{v}^{p}_{123}$.

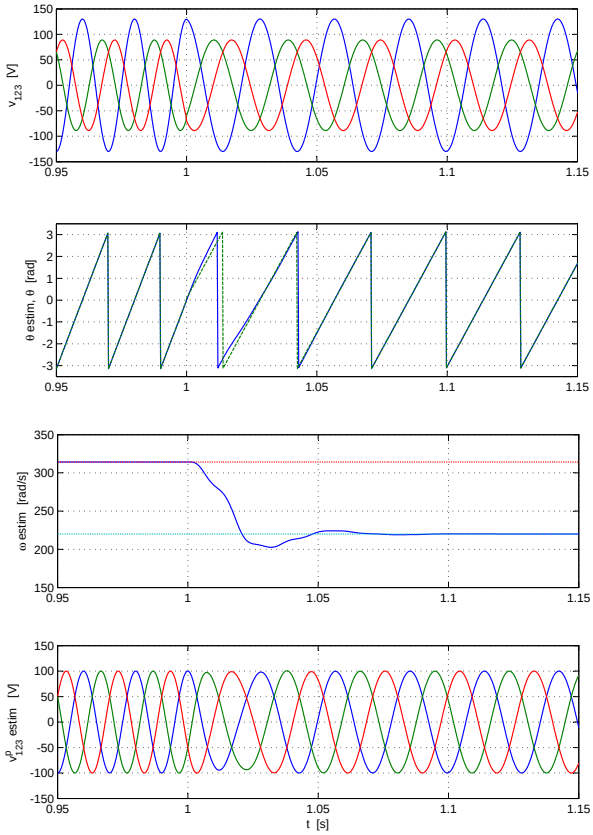

Figure 7.6: Depicts the transient response of the proposed FRF-PLL to a utility frequency change from 35 Hz to 50 Hz. (from top to bottom) Utility voltage v_{123}, estimated phase angle $\hat{\theta}$, estimated angular frequency $\hat{\omega}$, and estimated positive-sequence voltage in the synchronous reference frame $\hat{v}^{p}_{123}$.

(i) Balanced condition. The voltage source is formed only by a positive sequence and angular frequency of 50 Hz (314.16 rad/s), with a zero phase shift.

(ii) Unbalanced condition. The voltage source includes both a positive and a negative sequence components. For this purpose the input signals are considered as $\sqrt{3}v_\alpha = v_\beta$ with a phase angle of 150 degrees between them.

(iii) Utility frequency changes. Utility frequency chances from 40 Hz to 70 Hz and 70 Hz to 40 Hz.

Figure 7.7 depicts the response of the proposed FRF-PLL when the utility voltage has an unbalanced condition. Notice that both estimated positive-sequence voltages in the fixed reference frame, $\hat{v}^p_\alpha$ and $\hat{v}^p_\beta$, have equal amplitude.

Figure 7.8 depicts the response of the proposed FRF-PLL to an unbalanced highly distorted utility voltage. As in Fig.7.7, both estimated positive-sequence voltages have equal amplitude, and the response of the estimated angular frequency $\hat{\omega}$ does not show any distortion.

Figure 7.9 depicts the transient response of the proposed FRF-PLL when the utility voltage goes from a balanced to an unbalanced condition. Notice that both estimated positive-sequence voltages in the fixed reference frame, $\hat{v}^p_\alpha$ and $\hat{v}^p_\beta$, have equal amplitude, and as expected, the amplitude of both signals are reduced in the unbalanced case.

Figure 7.10 and Fig.7.11 depicts the transient response of the proposed FRF-PLL to a step change in the angular frequency of the source voltage going from 40Hz to 70Hz, and from 70Hz to 40Hz. In both figures, the estimated phase angle reach its desired value after a short transient. Notice also that, the estimated positive-sequence voltages maintain their amplitude after an almost imperceptible transient.

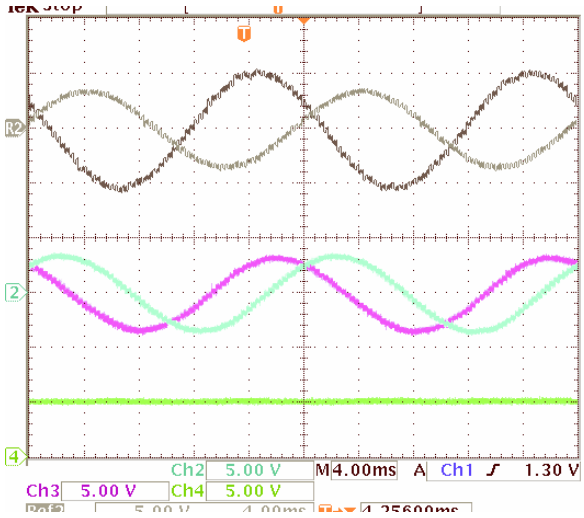

Figure 7.7: Depicts the response of the proposed FRF-PLL when the utility voltage has an unbalanced condition. (from top to bottom) Utility voltage $v_{\alpha\beta}$, estimated positive-sequence voltage in the fixed reference frame $\hat{v}^p_{\alpha\beta}$ and estimated angular frequency $\hat{\omega}$.

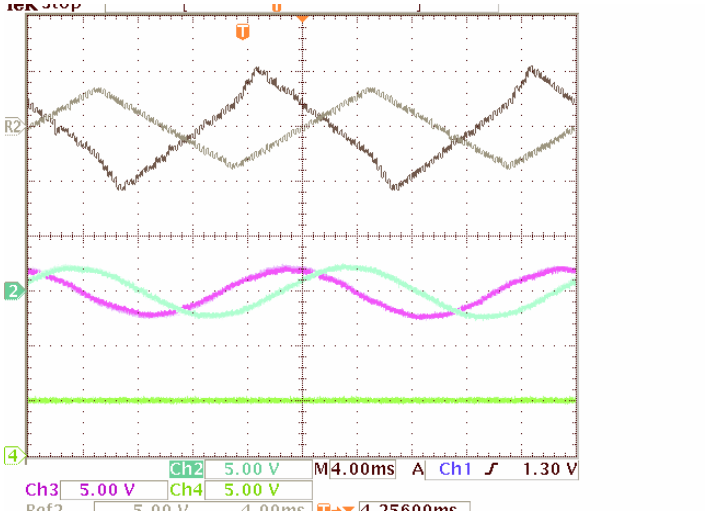

Figure 7.8: Depicts the response of the proposed FRF-PLL to an unbalanced highly distorted utility voltage. (from top to bottom) Utility voltage $v_{\alpha\beta}$, estimated positive-sequence voltage in the fixed reference frame $\hat{v}^p_{\alpha\beta}$ and estimated angular frequency $\hat{\omega}$.

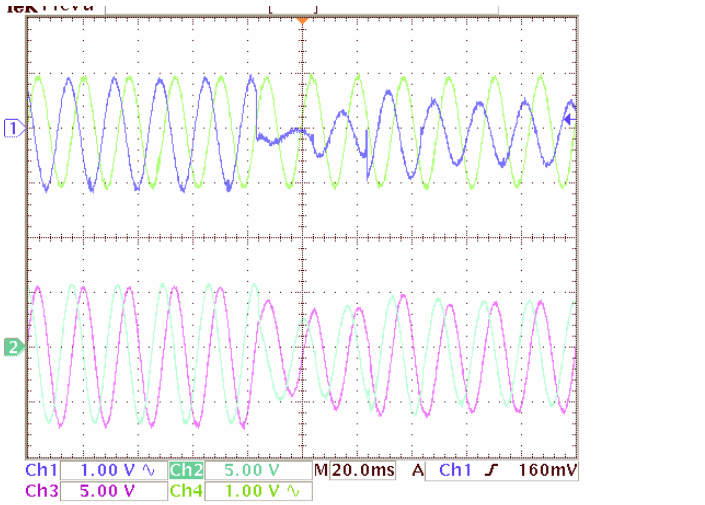

Figure 7.9: Depicts the transient response of the proposed FRF-PLL when the utility voltage goes from a balanced to an unbalanced condition. (top) Utility voltage $v_{\alpha\beta}$,and (bottom) estimated positive-sequence voltage in the fixed reference frame $\hat{v}^p_{\alpha\beta}$.

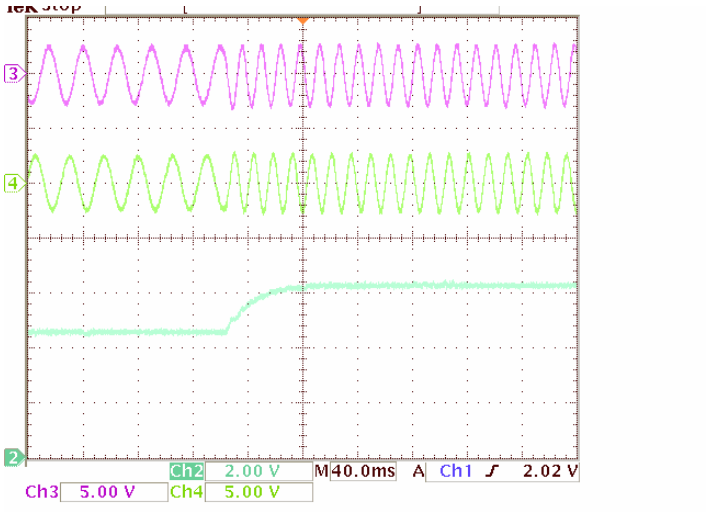

Figure 7.10: Depicts the transient response of the proposed FRF-PLL to a utility frequency change from 40 Hz to 70 Hz. (from top to bottom) Positive-sequence voltage v_α, positive-sequence voltage v_β, and estimated angular frequency $\hat{\omega}$.

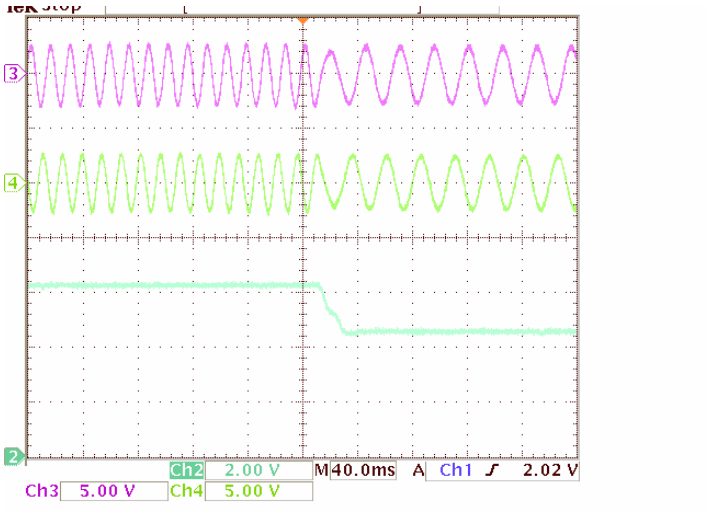

Figure 7.11: Depicts the transient response of the proposed FRF-PLL to a utility frequency change from 70 Hz to 40 Hz. (from top to bottom) Positive-sequence voltage v_α, positive-sequence voltage v_β, and estimated angular frequency $\hat{\omega}$.

7.7 Conclusions

In this chapter a PLL scheme was presented which is aimed to estimate the fundamental frequency, and both positive and negative sequences of the fundamental component of an unbalanced three-phase signal. The design process involved the proposal of a model that accurately reproduced the evolution of an unbalanced three-phase signal. For this purpose both positive and negative sequence components of the three-phase signal were considered. Based on the proposed model, a state estimator was designed to reconstruct both positive and negative sequences of the three-phase signal. The state estimator was built as a copy of the model with additional damping. An adaptation law was incorporated to reconstruct the angular frequency as well, which was involved in the state estimator. The proposed scheme delivers the estimates of both sequences in fixed frame coordinates, and does not require the transformation of variables to the synchronous reference frame as in most conventional PLLs. The proposed PLL was referred as fixed reference frame PLL (FRF-PLL), and was designed to properly operate under severe unbalanced conditions. It was shown that the proposed scheme was robust against angular frequency changes in the three-phase source voltage signal. Although not considered in the design, it was shown that the scheme was also robust against harmonic distortion present in the source voltage signal. For the stability and convergence study of the proposed FRF-PLL scheme, the Lyapunovs approach was followed without involving any linearization process. Also it was proposed an algorithm to tune the proposed FRF-PLL, which was based on the desired bandwidth frequency ω_{BW} of the frequency response of the linearized version of the proposed scheme. Numerical results and experimental results were presented and compared with the conventional SRF-PLL scheme to exhibit the benefits of the proposed FRF-PLL scheme over the conventional scheme, specially in the unbalanced case response.

Chapter 8

Conclusions, future research and scientific production

This thesis presented the mathematical models and the control laws of two main topologies of multilevel converters, namely, the diode clamped multilevel converter (NPC) and cascaded H-bridge multilevel converter (HB). It was found, regardless of the topology studied, that a natural way to write the model is considering as variables the sum and the difference of the capacitors voltages, besides the inductor currents. The key to solve the problem of balancing the capacitor voltages is precisely to consider variables that represent this difference in order to deal with it.

In comparison with other works in this area, this thesis is the only one that presents control laws based in mathematical models. It is true that in previous works [42], [43], [41], [70] are presented some mathematical models, but the control proposed in that works were not based in the mathematical models, and the most important thing, the model presented in that works not show how the control inputs deals directly with the balancing of the capacitor voltages.

Even when in that works were proposed Passivity-based controllers, energy-based controllers, control using Resultant Theory and others, the main contribution of this thesis is controllers that exploit the structure of the systems. All the controllers proposed in the thesis are designed to solve the problem of balancing the capacitor voltages, regardless of the application of rectifier or active filter.

It was also observed that in the single phase case, the mathematical models shows control inputs that affect directly to the balancing of the capacitor voltages, but in the three-phase cases, was not clear this input, with the exception of the three-level NPC converter, where the proposed model stressed the existence of a third degree of freedom (DOF) offered by the control input, and referred here as the γ-component. In Chapter 5 it has been highlighted that while the current tracking and regulation problems could be solved in a quite familiar way, the balancing of the capacitor voltages required a more involved process. In fact, it was shown that this balancing was possible after the introduction of extra control inputs that basically distorted the current reference. This distortion was, however, present during transients only, and vanishes in the steady state. The effectiveness of the proposed controller open the possibility to apply a similar process to other topologies of multilevel converters that present the problem of balancing, and whenever the number of explicitly available control

inputs is limited.

It is also presented in this thesis two new schemes of PLL for single phase and three phase systems. The proposed algorithms were designed based on the mathematical models of the input signals and were developed without involving any linearization process as in most conventional PLL schemes. It was show that with a complete description of the input signal, it is possible to design an algorithm to properly operate under severe unbalanced conditions (in the three-phase case) and also robust against harmonic distortion in the source voltage signal.

In the Chapter 7 a new PLL scheme was presented which is aimed to estimate the fundamental frequency, and both positive and negative sequences of the fundamental component of an unbalanced three-phase signal. The main contribution is that the proposed scheme delivers the estimates of both sequences in fixed frame coordinates, and does not require the transformation of variables to the synchronous reference frame as in most conventional PLLs. The proposed PLL was referred as fixed reference frame PLL (FRF-PLL).

Future research

This thesis work, opens a series of investigations in the field of multilevel converters, so it is necessary to set the points to follow in the future to allow an optimal use of this technology. In what follows there are some works to be done to follow up on this research topic.

- ▷ Based on the controller proposed for the cascade H-bridge three-phase multilevel converter, apply the same ideas to design a controller for the three-phase five-level NPC multilevel converter, which present also the issue of capacitor voltages balancing. The main reason to apply these technique to this topology is because the five-level NPC multilevel converter was already studied during the the thesis, and it was found that without an extra DOF, it is impossible to balance the capacitor voltages. The results for the three-phase HB multilevel converter opens the possibility to introduce an extra DOF using the structure of the system, and with already a mathematical model for the three-phase five-level NPC multilevel converter, is less difficult to explore this possibility.

- ▷ For the cascaded H-bridge multilevel converter there is a prototype almost ready for the programming of the proposed control laws. For this reason it is proposed to continue the study of this topology and obtain experimental results with the prototype mentioned.

- ▷ None of the proposed controllers in this thesis includes an scheme for the synchronization to the grid. The power electronics contributes to the efficient use of renewable energy and part of its application is linked to the development of new investigations within this field of electronics. For this reason it is proposed to include in the applications the PLL schemes designed in this thesis, in order to obtain a more efficient controller.

Even if the effectiveness of the FRF-PLL scheme in the unbalanced case has been put in evidence, its performance under harmonic distortion can still be improved. To follow up this,

it could be proposed to design an scheme based on a more complete model that in addition to the unbalance, it may also consider and reproduce the evolution of a distorted three-phase signal. To cope with the distortion in the signal, the scheme could include a better filtering of the harmonics, or include adaptation to cancel out such a distortion. It is very likely that such a harmonic mechanism relays in schemes such as a bank of resonant filters or simply a repetitive control. Similar ideas can be followed for the proposed single phase PLL, to cope with the harmonic distortion.

8.1 Scientific production

The following papers are directly related to this thesis work:

- G. Escobar, R.C. Portillo, M.F. Martínez-Montejano, E. Galván and J.M. Carrasco. "Modeling of a three-level neutral-point clamped converter," (submitted to IEEE Trans. Industrial Electronics).

- G. Escobar, M. F. Martínez-Montejano, P. R. Martínez-Rodríguez and M. Hernández-Gómez. "A model-based controller for the cascade h-bridge multilevel converter used as a shunt active filter", Proc. 37th IEEE Power Electronics Specialists Conference PESC'06, Jeju, Corea, 18-22 June 2006, pp. 1-5.

- G. Escobar, A.A. Valdéz, M.F. Martínez-Montejano and V.M. Rodríguez-Zermeo. "A model based controller for the cascade multilevel converter used as a shunt active filter", IEEE Industrial Applications Society Annual Meeting IAS'07, New Orleans, USA, September 23-27, 2007.

- M. F. Martínez-Montejano, Gerardo Escobar and Raymundo E. Torres-Olguín, "Fixed reference frame phase-locked loop (FRF-PLL) for unbalanced line voltage conditions", accepted in Proc. 39th IEEE Power Electronics Specialists Conference PESC'08, Rhodes, Greece, 15-18 June 2008.

- G. Escobar, M.F. Martínez-Montejano, R.E. Torres-Olguín, " Fixed reference frame phase-locked loop (FRF-PLL) for grid synchronization under unbalanced operation", (submitted to IEEE Trans. Industrial Electronics).

The following papers are indirectly related to this thesis work:

- G. Escobar, A. A. Valdéz, R.E. Torres-Olguín and M. F. Martínez-Montejano. "A model-based controller for a three-phase four-wire shunt active filter with compensation of the neutral line current", IEEE Trans. on Power Electronics, Vol. 22, No. 6, pp. 2261-2270, Nov. 2007.

- G. Escobar, M. H. Gómez, P.R. Martínez and M. F. Martínez-Montejano, "A repetitive-based controller for a power factor precompensator", IEEE Trans. On Circuits and Systems. Vol. 54, No. 9, pp.: 1968-1976, September 2007.

- G. Escobar, P.R. Martínez, A.A. Valdéz, J. Leyva-Ramos, and M. F. Martínez, "A repetitive-based controller to compensate for harmonic distortion in the output voltage of a boost converter", Proc. 36th IEEE Power Electronics Specialists Conference PESC'05, Recife, Brazil, 11-16 June 2005, pp. 2709-2715.

- G. Escobar, J. Leyva-Ramos, P.F. Martínez, M. F. Martínez, "A repetitive-based controller for a shunt active filter to compensate for reactive power and harmonic distortion", 44th IEEE Conference on Decision and Control CDC-EDC05, Sevilla, Spain, 12-15 December 2005, pp. 6480-6485.

- G. Escobar, M. F. Martínez-Montejano, P. R. Martínez-Rodríguez and M. Hernández-Gómez. "A model-based controller for the cascade h-bridge multilevel converter used as a shunt active filter", Proc. 37th IEEE Power Electronics Specialists Conference PESC'06, Jeju, Corea, 18-22 June 2006, pp. 1-5.

- G. Escobar, A.A. Valdéz, R.E. Torres-Olguín, M. F. Martínez-Montejano "Repetitive-based controller in stationary reference frame for D-Statcom in unbalanced operation", 2006 IEEE International Symposium on Industrial Electronics, ISIE'2006, Montral, Canada, Vol. 2, July 9 to 13, 2006, pp. 1388-1393.

- P.R. Martínez-Rodríguez, G.Escobar, M. Hernández-Gómez, R.E. Torres-Olguín, M. F. Martínez Montejano. "Power factor correction with an active filter using a repetitive controller", 2006 IEEE International Symposium on Industrial Electronics, ISIE'2006, Montral, Canada, Vol. 2, July 9 to 13, 2006, pp. 1394-1399.

- G. Escobar, A.A. Valdéz, R.E. Torres-Olguín, M. F. Martínez-Montejano, "A model-based controller for a three-phase four-wire shunt active filter with compensation of the neutral line current", 10th IEEE International Power Electronics Congress, CIEP'06, Oct, 2006, pp. 1-6.

- G. Escobar, A.A. Valdéz, M. F. Martínez-Montejano and V.M. Rodríguez-Zermeo. "A model based controller for the cascade multilevel converter used as a shunt active filter", IEEE Industrial Applications Society Annual Meeting IAS'07, New Orleans, USA, September 23-27, 2007.

- M. F. Martínez-Montejano, Gerardo Escobar and Raymundo E. Torres-Olguín, "Fixed reference frame phase-locked loop (FRF-PLL) for unbalanced line voltage conditions", accepted in Proc. 39th IEEE Power Electronics Specialists Conference PESC'08, Rhodes, Greece, 15-18 June 2008.

- G. Escobar, M. F. Martínez-Montejano and R. E. Torres-Olguín, "An adaptive direct power control for three-phase PWM rectifier in the unbalanced case", accepted in Proc. 39th IEEE Power Electronics Specialists Conference PESC'08, Rhodes, Greece, 15-18 June 2008.

- A. A. Valdéz, G. Escobar and M. F. Martínez-Montejano, "A model-based controller for a hybrid power filter to compensate harmonic distortion in unbalanced operation", accepted in Proc. 39th IEEE Power Electronics Specialists Conference PESC'08, Rhodes, Greece, 15-18 June 2008.

Two patents are directly related to this thesis work:

- G. Escobar, M. F. Martínez-Montejano, A. A. Valdéz, and R. E. Torres-Olgun, ”Controller For The Three-Phase Cascade Multilevel Converter Used As Shunt Active Filter In Unbalanced Operation With Guaranteed Capacitors Voltages Balance”, U.S. PTO Appl. No. 11975231, December 2007.
- G. Escobar, M. F. Martínez-Montejano, and R. E. Torres-Olguín, ”Fixed Reference Frame Phase-Locked Loop (Frf-Pll) For Unbalanced Line Voltage Conditions.” U.S. PTO Appl. No. 11977023, December 2007.

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