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# A SIMPLE CIRCUIT WITH DYNAMIC LOGIC ARCHITECTURE OF BASIC LOGIC GATES

I. CAMPOS CANTÓN and J. A. PECINA-SÁNCHEZ

*Facultad de Ciencias, Universidad Autónoma de San Luis Potosí,  
Alvaro Obregón 64, 78000, San Luis Potosí, SLP, México*

E. CAMPOS CANTÓN

*Departamento de Físico Matemáticas,  
Universidad Autónoma de San Luis Potosí,  
Alvaro Obregón 64, 78000, San Luis Potosí, SLP, México and  
Instituto Potosino de Investigación Científica y Tecnológica,  
Camino a la presa San José 2055,  
78216, San Luis Potosí, SLP, México*

H. C. ROSU

*Instituto Potosino de Investigación Científica y Tecnológica,  
Camino a la presa San José 2055,  
78216, San Luis Potosí, SLP, México*

We report experimental results obtained with a circuit possessing dynamic logic architecture based on one of the theoretical schemes proposed by H. Peng and collaborators in 2008. The schematic diagram of the electronic circuit and its implementation to get different basic logic gates are displayed and discussed. In particular, we show explicitly how to get the electronic NOR, NAND, and XOR gates. The proposed electronic circuit is easy to build because it employs only resistors, operational amplifiers and comparators.

*Keywords:* chaos computing, analog electronic, piecewise-linear functions.

## 1. Introduction

There is great interest in developing new working paradigms in order to complement and even replace the present statically-wired computer architectures. One of the frontier ideas put forth by Sinha and Ditto in 1998 [Sinha & Ditto, 1998] is to get new devices with a dynamic logic architecture that now is called chaos computing because chaotic (non-linear) elements are employed to get the logic operations [Sinha & Ditto, 1999; Kuo, 2005; Munakata *et al.*, 2002]. The main task in this case is to achieve logic gates (also called cells here) that are able to change their response according to the control parameter and reconfiguring the device in order to obtain whatever logic gate. These dynamic logic gates give us the possibility to build logic chips for the next generation of computers. Moreover, Sinha and Ditto [Sinha & Ditto, 1999] extended their proposal to encode numbers, perform specific arithmetic operations such as addition and multiplication, and so on. In a theoretical work of Kuo [Kuo, 2005] the logistic map was used as the chaotic element and employed to emulate logic gates. Currently, there is stimulating research activity in exploiting the logic features of the nonlinear dynamical systems through their electronic implementations [Murali *et al.*, 2009; Murali *et al.*, 2009; Murali *et al.*, 2005; Murali *et al.*, 2003].

The goal of this work is to present some experimental results that we obtained by means of a simple electronic circuit with dynamic logic architecture. The circuit was designed based on the first of the three theoretical schemes reported by Peng and collaborators in order to build dynamic logic gates [Peng *et al.*, 2008]. The electric diagram of that scheme is easy to implement in our electronic circuit and the employed components can be acquired in any electronic store.

## 2. Electronic Dynamical Logic Gate

The discrete dynamical system used in [Peng *et al.*, 2008] to simulate dynamic logic gates is the following:

When $K \in$ :	The cell is:
$[0, C - \beta]$	NOR
$(C - \beta, \beta)$	NAND
$[\beta, 2C - \beta]$	XOR
$(2C - \beta, C + \beta)$	OR
$[C + \beta, 2C]$	AND

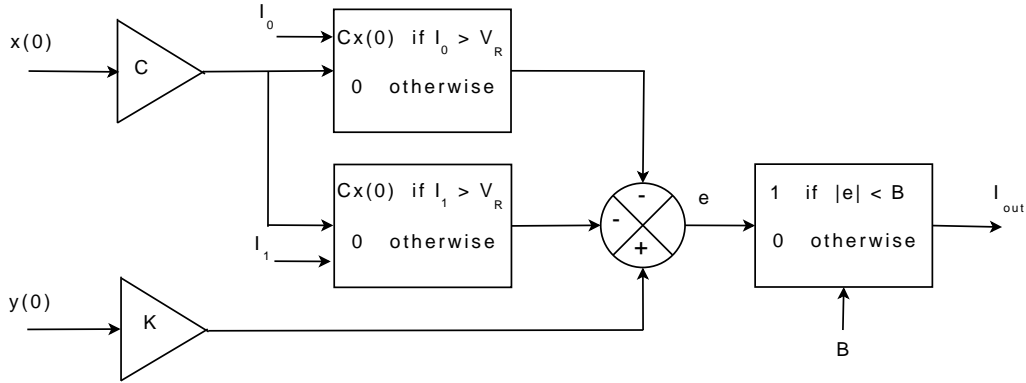
**Table I:** The ranges of the parameter  $K$  for which the system (1) behaves like the corresponding basic logic gates in the second column.

$$\begin{aligned}
x(n+1) &= C(I_0 + I_1)x(n) \\
y(n+1) &= Ky(n) \\
I_{out} &= \begin{cases} 1, & \text{if } |y(m) - x(m)| < \beta \\ 0, & \text{otherwise,} \end{cases}
\end{aligned} \tag{1}$$

where  $C$  and  $\beta$  are positive constants,  $K$  is the bifurcation parameter which acts as the logic-gate controller,  $m$  is the number of iterative steps,  $I_0$  and  $I_1$  are the input logic signals, and  $I_{out}$  is the output signal.

The dynamic logic gate given by equation (1) is controlled through the  $K$  parameter according to the intervals given in table I and restricted to  $\frac{C}{2} < \beta \leq C$ ,  $m = 1$ , see [Peng *et al.*, 2008].

The block diagram of the electronic circuit of the dynamic logic gate is shown in Fig. 1. The simplicity of this circuit is due to the fact that the linear mathematical operation of commutation is performed by the comparators in the switching blocks, as is shown in Fig. 1. The first switching block checks if the input  $I_0$  is a 0V or 5V and generates an output equal to 0V or  $Cx(0)$ , respectively. The second switching block does the same for the input  $I_1$ . With the outputs of the two switching blocks and the input  $y(0)$  the input  $e = |y(1) - x(1)|$  of the third switching block is estimated in order to produce the output  $I_{out}$  of the logic gate. The schematic diagram of the dynamic logic gate circuit is shown in Fig. 2. It consists of eight operational amplifiers (from U1 to U8), four comparators (U9 - U12), 21 resistors (from R1 to R21), and two potentiometers  $k_1$  and  $k_2$ . Assuming ideal performance from all components, the circuit in Fig. 2 is modelled by the following set of equations in the nodes



**Fig. 1:** Block diagram of the dynamic logic gate.

labelled as d, f, g and h. For the node d,

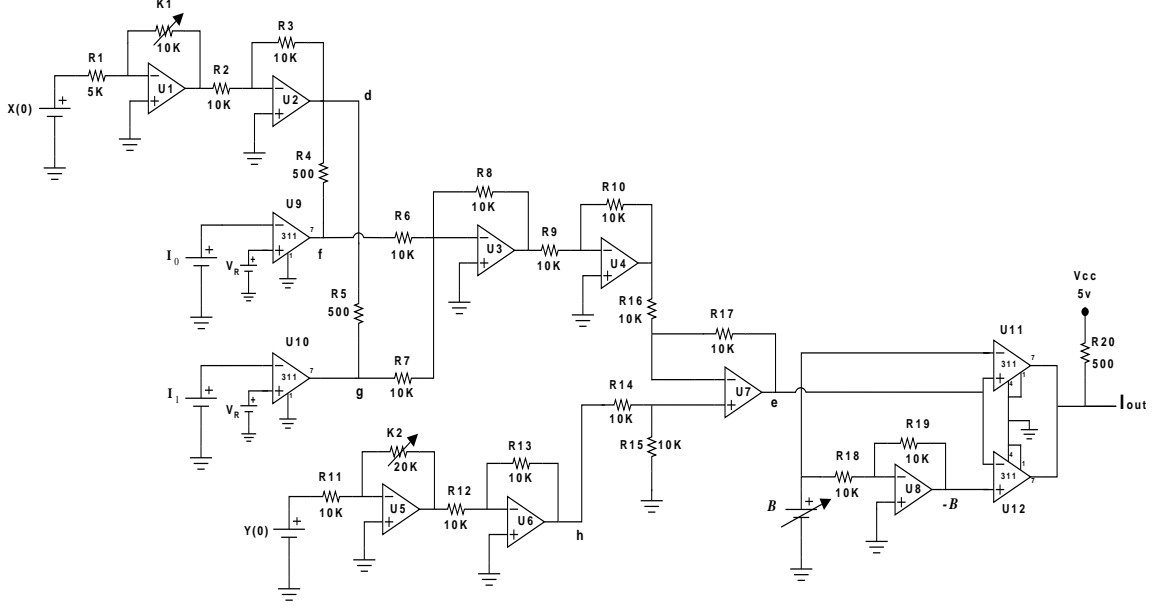
$$d = -\frac{R_3 k_1}{R_2 R_1} x(0) . \quad (2)$$

The voltages in the nodes f and g are given as follows

$$f = \begin{cases} d & \text{if } I_0 > V_R, \\ 0 & \text{if } I_0 \leq V_R, \end{cases} \quad g = \begin{cases} d, & \text{if } I_1 > V_R, \\ 0, & \text{if } I_1 \leq V_R, \end{cases} \quad (3)$$

while the voltage at the node h is given by

$$h = \frac{k_2 R_{14}}{R_{12} R_{13}} y(0) . \quad (4)$$



**Fig. 2:** Schematic diagram of the dynamic logic gate electronic circuit.

Combining now the equations for the nodes d, f, g, and h one can get the voltage in the node e

$$e = \left( \frac{1 + \frac{R_{18}}{R_{17}}}{1 + \frac{R_{15}}{R_{16}}} \right) h - \frac{R_{18}R_{11}}{R_{17}R_{10}} \left( \frac{R_9}{R_7} f + \frac{R_9}{R_8} g \right). \quad (5)$$

Lastly, the outputs of comparators  $U_{11}$  and  $U_{12}$  as functions of the voltage in the node e are

$$U_{11_0}(e) = \begin{cases} v_{cc}, & \text{if } \beta > e, \\ 0, & \text{otherwise.} \end{cases} \quad U_{12_0}(e) = \begin{cases} v_{cc}, & \text{if } e > -\beta, \\ 0, & \text{otherwise.} \end{cases} \quad (6)$$

Relating the equations (2) to (6) and taking the values for the components given in Table II one can get the output voltage of the circuit. As a function of  $I_0$  and  $I_1$ , it is given by the following set of equations:

Components	Value
Resistors: $R_{1,12}$	1 $k\Omega$
Resistors: $R_{2,3,7,8,9,10,11,13,14,15}$	10 $k\Omega$
Resistors: $R_{5,6,21}$	500 $\Omega$
Potentiometer: $k_1$	10 $k\Omega$
Potentiometer: $k_2$	20 $k\Omega$
Op. Amplifiers: $U_{1,\dots,8}$	TL081
Comparators: $U_{9,\dots,12}$	LM311

**Table II:** The electronic components and their values as employed in the construction of the dynamic logic gate electronic circuit.

$$e = \begin{cases} Ky(0) - 2Cx(0), & \text{if } I_0, I_1 > V_R, \\ Ky(0) - Cx(0), & \text{if } I_0 > V_R \ \& \ I_1 \leq V_R \ \text{or} \ I_1 > V_R \ \& \ I_0 \leq V_R, \\ Ky(0), & \text{otherwise,} \end{cases} \quad (7)$$

where  $K = \frac{k_2}{R_{12}}$  and  $C = \frac{k_1}{R_1}$ .

$$I_{out} = \begin{cases} v_{cc}, & \text{if } |e| < \beta, \\ 0, & \text{otherwise.} \end{cases} \quad (8)$$

### 3. Experimental Results

The initial conditions  $x(0)$  and  $y(0)$  were taken equal to 1 V. The inputs  $I_0$  and  $I_1$  of the dynamic logic gate take only two values 0 V and 5 V in order to represent the binary values 0 and 1, respectively. The voltage  $V_R = 1$  V is the transition voltage between 0 V (logic 0) and 5 V (logic 1). The different basic logic gates were obtained varying the value of the potentiometer  $k_2$  at fixed value of the potentiometer  $k_1$ , e.g., for a given value of the potentiometer  $k_1$ , tuning the value of the potentiometer  $k_2$  is required in order to get the desirable logic gate. The value of  $\beta$  is adjusted by means of a variable source. We implemented this design on a printed circuit board (PCB) manufactured in our laboratory. In the

When $K \in$ :	The circuit behaves as the following gate:
$[0, 0.25]$	NOR
$(0.25, 0.75)$	NAND
$[0.75, 1.25]$	XOR
$(1.25, 1.75)$	OR
$[1.75, 2]$	AND

**Table III:** The intervals of the parameter  $K$  and the corresponding basic logic gate of the circuit .

experimental circuit, we used the TL081 operational amplifiers and the LM311 comparators supplied with a power source at  $\pm 15V$  and soldered directly to the PCB without a socket. The voltage  $V_{dc}$  was supplied by a variable dc supply source with an output range of 0 - 15V.

We show now how to obtain the different kinds of basic logic gates. For example, if the potentiometer  $k_1$  is equal to the resistor  $R_1$  then  $C = 1$ , and fixing the voltages of  $\beta$  to 0.75V, we get  $x(0) = 1V$  and  $y(0) = 1V$ . Equations (5) and (6) can be rewritten as follows

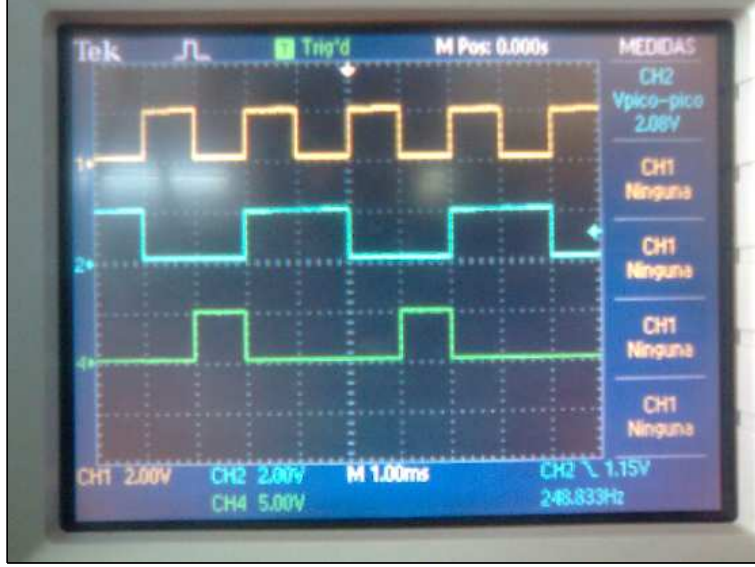
$$e = \begin{cases} K - 2, & \text{if } I_0, I_1 > 1V, \\ K - 1 & \text{if } I_0 > 1V \ \& \ I_1 \leq 1V \ \text{or } I_1 > 1V \ \& \ I_0 \leq 1V, \\ K, & \text{otherwise.} \end{cases} \quad (9)$$

$$I_{out} = \begin{cases} 5V, & \text{if } |e| < 0.75, \\ 0V, & \text{otherwise.} \end{cases} \quad (10)$$

The parameter  $K$  is controlled by the potentiometer  $k_2$  and the intervals according to the values of the parameters  $\beta$  and  $C$  are given in Table III.

We analyze three different cases for the parameter  $K$  corresponding to  $k_2 = 200\Omega$ ,  $500\Omega$  and  $1k\Omega$ , but other cases can be investigated in the same way. These values fix the value of  $K$  to 0.2, 0.5 and 1, respectively.





**Fig. 3:** The two input signals and the output signal of the NOR gate as seen on the oscilloscope screen.

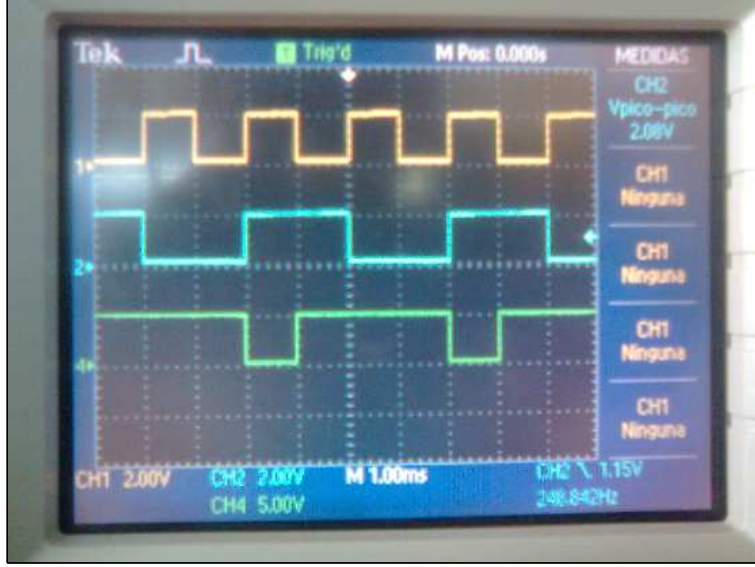
For  $K = 0.2$ , we have the following response in the node  $e$

$$e_{0.2} = \begin{cases} -1.8, & \text{if } I_0, I_1 > 1V, \\ -0.8 & \text{if } I_0 > 1V \ \& \ I_1 \leq 1V \ \text{or} \ I_1 > 1V \ \& \ I_0 \leq 1V, \\ 0.2, & \text{otherwise.} \end{cases} \quad (11)$$

The output given by equation (10) and taking the input given by equation (12) yields the following table

$I_1(V)$	$I_0(V)$	$e(V)$	$I_{out}(V)$
0	0	0.2	5
0	5	-0.8	0
5	0	-0.8	0
5	5	-1.8	0

Considering that 0V is a logic zero and 5V is a logic one, then according to the inputs  $I_0, I_1$  and the output  $I_{out}$  the dynamic logic gate behaves as a NOR gate as can be seen in Fig. 3.



**Fig. 4:** The two input signals and the output signal of the NAND gate as seen on the oscilloscope screen.

$K = 0.5$  corresponds to the interval of the NAND gate, see Table III. Then, we have

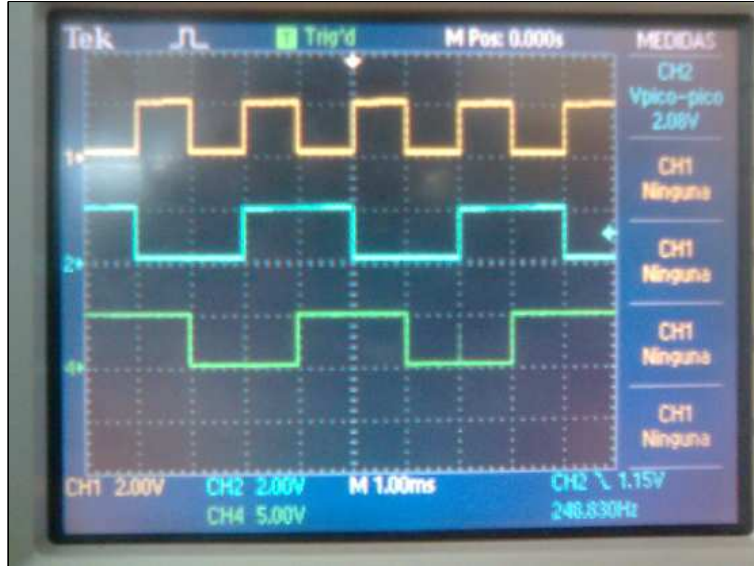
$$e_{0.5} = \begin{cases} -1.5, & \text{if } I_0, I_1 > 1V, \\ -1.5 & \text{if } I_0 > 1V \text{ \& } I_1 \leq 1V \text{ or } I_1 > 1V \text{ \& } I_0 \leq 1V, \\ 0.5, & \text{otherwise.} \end{cases}$$

$I_1(V)$	$I_0(V)$	$e(V)$	$I_{out}(V)$
0	0	0.5	5
0	5	-0.5	5
5	0	-0.5	5
5	5	-1.5	0

(12)

For this case, the experimental input-output signals of the NAND gate are shown in Fig. 4.

For  $K = 1$ , we have the dynamic logic gate behaving as a XOR gate. The input and



**Fig. 5:** The two input signals and the output signal of the XOR gate as seen on the oscilloscope screen.

output of the circuit are shown in the next equation and table

$$e_1 = \begin{cases} -1, & \text{if } I_0, I_1 > 1V, \\ 0 & \text{if } I_0 > 1V \text{ \& } I_1 \leq 1V \text{ or } I_1 > 1V \text{ \& } I_0 \leq 1V, \\ 1, & \text{otherwise.} \end{cases}$$

$I_1(V)$	$I_0(V)$	$e(V)$	$I_{out}(V)$
0	0	0	0
0	5	0	5
5	0	0	5
5	5	-1	0

(13)

The experimental results are presented in Fig. 5.

The other logic gates can be checked in the same way for the different values of the parameter  $K$ .

## 4. Conclusions

A very simple dynamic logic gate electronic circuit has been described here together with its implementation using only analog components such as operational amplifiers, comparators and resistors. Its experimental behavior was tested and compared with the numerical behavior given by the mathematical model of the dynamical logic gate that has been taken from the work of Peng and collaborators [Peng *et al.*, 2008]. Choosing different values of the potentiometer  $k_2$  offers us the possibility to get different logic gates: NOR, NAND, XOR, and others. Such circuit realizations have many potential applications in chaos computing. Finally, we notice that our design can be manufactured in just one chip because the final electronic circuit contains only semiconductors and passive components.

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