The Delayed Quadratic Buck Converter

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Abstract: Nowadays, the microprocessors family normally require for the input source not only low voltage but also high current. There exists an increasing necessity for developing new applied techniques on topologies and control strategies, which may be able to full fill such requirements. Although a considerable amount of applications use the conventional buck converter for step-down for DC/DC conversion, when a high step-down conversion is required is a much better choice to implement the quadratic buck converter; however, the problem for obtaining a high step-down conversion at wide duty ratio still remains.
This document proposes the delayed quadratic buck converter, which offers a very high-step-down dc-dc conversion with a wide duty cycle. The quadratic buck converter is modified in its topology by adding an inductor, which allows us to obtain for the duty cycle a higher increment than this normally obtained by a quadratic one.
Converter behaviour and analysis are illustrated. Experimental results are also shown for a conversion from 36 V to 1.5 V and an output power of 20W.

1. Introduction

The conventional buck converter dominates the power-supply market in the Telecom and Datacom fields, not only, due to its simplicity in structure and low cost, but also, due to its capacity of step-down DC/DC conversion ratio when non-galvanic isolation is required. However, the new microprocessor power supplies demand high step-down conversion ratio, where output voltage normally varies from 3.3V to 1.1V, or even smaller range of values [1-3].

The duty ratio becomes very small when a lower output voltage is required. The power MOSFETs has a considerable gate capacitance, which must be charged beyond a threshold voltage in order to achieve the turn-ON. This process for charging the gate capacitance is provided by the gate driver, which has to fulfill its purpose within the period of time required by the system design. Under the circumstance, that the gate driver faces a switching difficulty between OFF and ON in short periods, it has been established a commitment between the regulation and the transitory response. Normally, the regulation becomes worse

in high-frequency applications, and the pulse-width modulation (PWM) has serious limitations on the minimum controllable ON-time. Hence, it is difficult to maintain the circuit control with a duty ratio with less than 10 % at high switching frequencies.

There exist topologies capable for avoiding the small duty ratio; these use transformers, capacitors and/or multistage converters [4-12]. According to literature [13], the system may also operate at two stages, on the first hand may include a conventional buck converter and, on the second hand an isolated converter, which may operate under 50% of the duty ratio. However, the required space, the losses, and the controller design, which are difficult to implement have become the main disadvantage for this proposal. Some other publications [14-15] suggest implementing a tapped-inductor buck converter, which has the disadvantage of introducing parasitic elements due to magnetic coupling, so that, more elements should be incorporated in order to alleviate this issue.

The quadratic buck converter (QBC) combines two conventional buck converters distributed in cascade using an active single switch [16-17], as shown in Figure 1. The conversion ratio is a quadratic function, as described here next:

$$\frac{V_o}{E} = D^2 \tag{1}$$

Where: E is the input voltage,

V_o is the output voltage, and

D is the duty cycle.

This last converter has the advantage of using an active single switch; even for the quadratic buck converter, the duty ratio is too small when a very low output voltage is required. The literature has proposed [18]-[19], converter with the aid of a multiplier in order to alleviate this problem, however, many components are required.

A synchronous rectifier may replace the freewheeling diode in order to reduce not only the conduction loss, but also to increase the efficiency considerably. According to the literature [20-22], this last

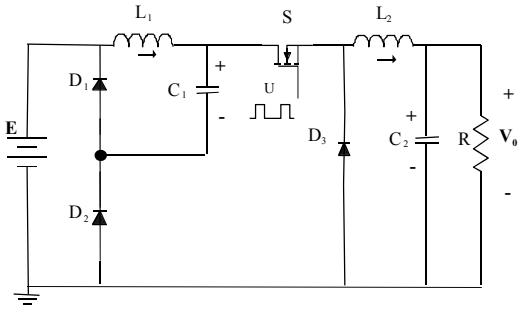


Fig. 1. *Traditional Quadratic Buck Converter*

configuration is better known as the synchronous rectifier quadratic buck converter. The conduction time for the main MOSFET is smaller compared to the freewheeling diode, which, it means that the conduction losses reach high values. When a synchronous rectifier is employed, the voltage across its terminals is lower than the freewheeling diode; therefore, the losses are reduced.

This paper proposes a topology based on the quadratic buck converter, where a high step-down conversion ratio is obtained, with a wider ratio, by adding a simple inductor to the topology

The paper is organized as follows: the proposed Delayed Quadratic Buck Converter (DQBC) is addressed in section two, where, operation, waveforms, and analysis for this converter are also included. In section three the performance of the converter is discussed. Experimental results are discussed in section four, and finally, some conclusions are given.

2. The delayed quadratic buck converter

The proposed converter is shown in Fig. 2. This topology is based on the quadratic buck converter, where a single inductor has been added. This simple inductor allows obtaining very high step-down conversion ratio with a wide duty ratio.

This proposal delays the voltage pulse applied to the second-stage output filter, and then a low output voltage may be obtained with a wider duty cycle. The desired duty cycle at a specific operating point may be determined by choosing properly the added inductor.

2.1. Operation of the converter

The converter waveforms are illustrated in Figure 3. The description for the circuit is focused on the main switch. The different stages are established by the main switch and the added inductor L_D.

- During $0 - t_1$. The main switch is turned 'on'. At this time the diodes D_2 and D_3 are conducting, the equivalent circuit is shown in Figure 4.a. The inductor L_D current (i_{LD}) is increased until this current plus the current of L_1 (i_{L1}) is equal to the inductor output current (i_{L2}).

  The voltage applied during this period to the output filter (L_2 and C_2) is still zero in spite of the main switch is "on" due to the diode D_3 is in conduction. The voltage applied to the filter is delayed due to the inductor L_D. The inductor L_1 current is increased, while the inductor L_2 current is decreased

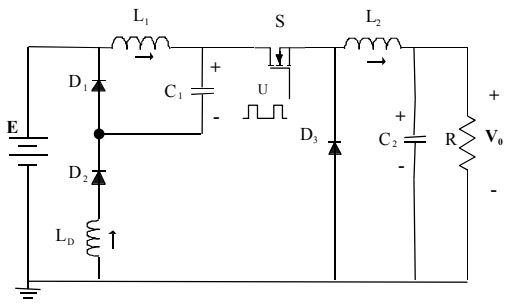


Fig. 2. *Delayed Quadratic Buck Converter*

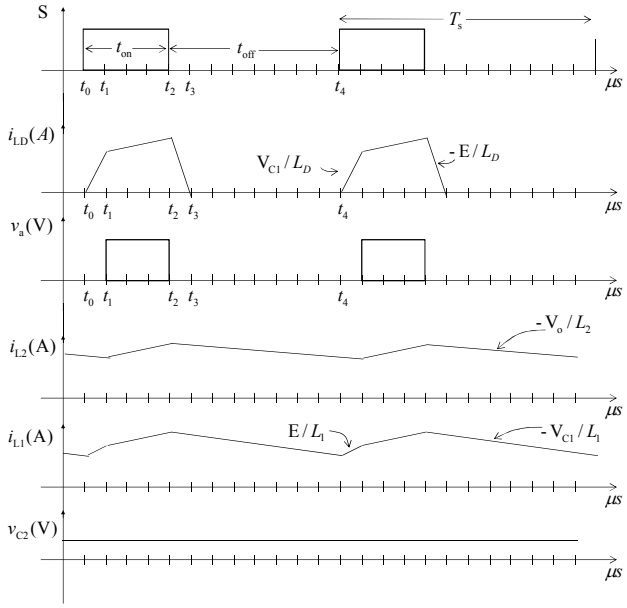


Fig. 3. *Waveforms of the Proposed Converter*

The time in this stage is mainly determined by L_D and the output current.

- During $t_1 - t_2$. The main switch is still 'on'. This stage starts once the current of inductor L_D reach the condition $i_{LD} = i_{L2} - i_{L1}$, then the diode D_3 is not conducting, only D_2 does; the equivalent circuit is shown in Figure 4.b. This stage is similar in operation to the traditional quadratic buck converter, with the only difference that exists L_D.

  A voltage is applied to the output filter (V_a), also the inductor L_1 and L_2 currents are increased.

  It should be noted that this stage establishes the actual duty cycle seen by the output filter. This stage and the previous one establish the duty cycle of the main switch. This means that the inductor L_D delays the duty cycle seen by the output filter, which allows us to have a lower gain with a higher duty cycle of the main switch compared to the traditional quadratic buck converter.

- During $t_2 - t_3$. The main switch is turned 'off'. At this time the three diodes D_1, D_2 and D_3 are conducting; the equivalent circuit is illustrated in Figure 4.c. The inductor L_D current (i_{LD}) is decreased until it reaches zero value.

  On this period of time, the voltage applied to the output filter (L_2 and C_2) is zero, since diode D_3 is in conduction. The inductor L_1 current is decreased, and it occurs the same for the inductor L_2 current.

  The time in this stage is mainly established by L_D and the input voltage.

- During $t_3 - T_s$. The main switch is still 'off'. At this time the diodes D_1 and D_3 are conducting; the equivalent circuit is shown in Figure 4.d. The inductor L_D (i_{LD}) has no current.

  Similar to the previous stage during this time the voltage applied to the output filter (L_2 and C_2) is

zero because the diode D_3 is in conduction. The inductor L_1 current is decreased, and it also occurs the same for the inductor L_2 current.

The inductors L_1 and L_2 are operated in continuous conduction mode (CCM), however the inductor L_D may be considered that operate in discontinuous conduction mode (DCM), this is explained because not only its current starts at zero at the beginning of the switching cycle, but also it reaches the zero current before the switching cycle ending.

The converter may be also operated completely in DCM, however, this would increase the losses, the analysis, in such circumstances, is beyond the purpose of this paper

2.2. On the analysis of the converter

The converter is analyzed considering each switching state by applying the averaging method [23-27]. Analysis from Figure 3 and 4, the next equations are obtained.

For t_0 to t_1 is obtained:

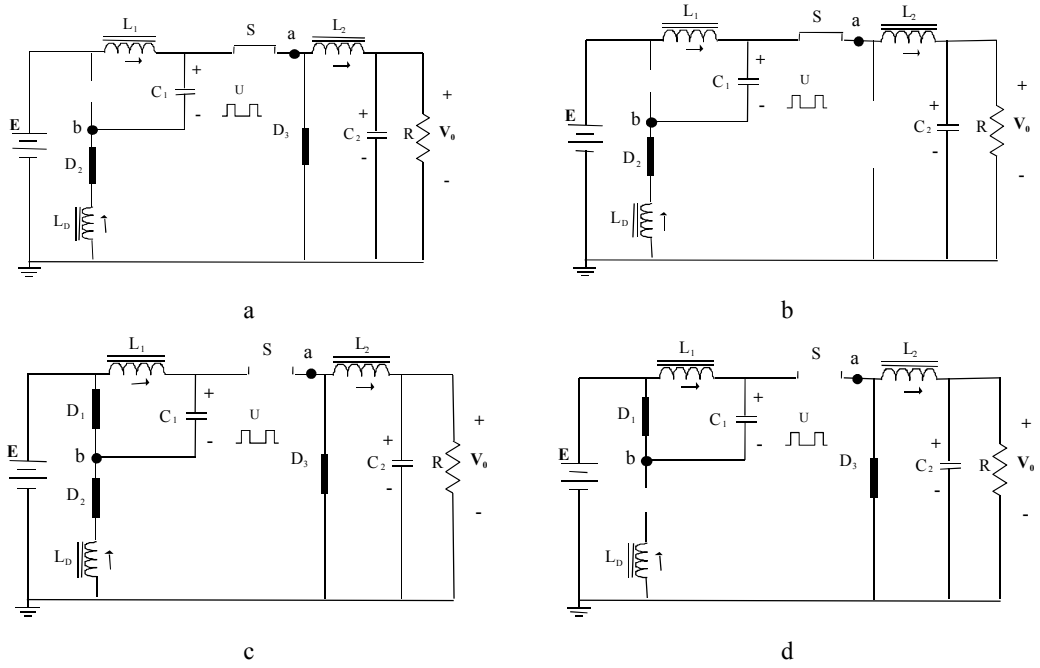


Fig. 4. *Subcircuits of the proposed converter*
a Circuit during $t_0 - t_1$
b Circuit during $t_1 - t_2$
c Circuit during $t_2 - t_3$
d Circuit during $t_3 - t_4$

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= E \\ L_2 \frac{di_{L2}}{dt} &= -v_{C2} \\ L_D \frac{di_{LD}}{dt} &= v_{C1} \\ C_1 \frac{dv_{C1}}{dt} &= -i_{LD} \\ C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \tag{2}$$

For t_1 to t_2 is obtained:

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= E - v_{C1} + L_D \frac{di_{Ld}}{dt} \\ L_2 \frac{di_{L2}}{dt} &= -v_{C2} + v_{C1} - L_D \frac{di_{Ld}}{dt} \\ C_1 \frac{dv_{C1}}{dt} &= -i_{LD} \\ C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \tag{3}$$

In this stage also the next equation is obtained:

$$i_{L1} + i_{LD} - i_{L2} = 0 \tag{4}$$

Using the first two terms of (3), equation (4), and after some algebraic manipulations is obtained:

$$L_D \frac{di_{LD}}{dt} = \frac{1}{L_r}\left(-E + \left(1 + \frac{L_1}{L_2}\right)v_{C1} - \frac{L_1}{L_2} v_{C2}\right) \tag{5}$$

Where: $\frac{1}{L_r} = \frac{L_D L_2}{L_1 L_2 + L_D L_2 + L_1 L_D}$

Considering (4) and (5), the equation (3) becomes:

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= \left(1 - \frac{1}{L_r}\right)E - \left(1 - \frac{1}{L_r} - \frac{L_1}{L_r L_2}\right)v_{C1} - \frac{L_1}{L_r L_2} v_{C2} \\ L_2 \frac{di_{L2}}{dt} &= \frac{1}{L_r} E + \left(1 - \frac{1}{L_r} - \frac{L_1}{L_r L_2}\right)v_{C1} + \left(\frac{L_1}{L_r L_2} - 1\right)v_{C2} \\ L_D \frac{di_{LD}}{dt} &= -\frac{1}{L_r} E + \left(\frac{1}{L_r} + \frac{L_1}{L_r L_2}\right)v_{C1} - \frac{L_1}{L_r L_2} v_{C2} \\ C_1 \frac{dv_{C1}}{dt} &= i_{L1} - i_{L2} \\ C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \tag{6}$$

For t_2 to t_3 is obtained:

$$\begin{aligned} L_1\frac{di_{L1}}{dt} &= -v_{C1} \\ L_2\frac{di_{L2}}{dt} &= -v_{C2} \\ L_D\frac{di_{LD}}{dt} &= -E \\ C_1\frac{dv_{C1}}{dt} &= i_{L1} \\ C_2\frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \tag{7}$$

For t_3 to t_4 is obtained:

$$\begin{aligned} L_1\frac{di_{L1}}{dt} &= -v_{C1} \\ L_2\frac{di_{L2}}{dt} &= -v_{C2} \\ L_D\frac{di_{LD}}{dt} &= 0 \\ C_1\frac{dv_{C1}}{dt} &= i_{L1} \\ C_2\frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \tag{8}$$

A reduced order system is obtained because L_D is operating in DCM [17],[26], by modeling with the reduced order averaging method. The inductor L_D does not store energy in a switching cycle, because, the variable starts and ends at zero current, mainly due to this reason, the variable does not qualify as a state variable in the average model.

Considering the previous equations, the piecewise linear model for the system variables are:

$$L_1\frac{di_{L1}}{dt} = \begin{cases} E & \forall\, t_0 \le t < t_1 \\ \left(1-\frac{1}{L_r}\right)E - \left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)v_{C1} - \frac{L_1}{L_rL_2}v_{C2} & \forall\, t_1 \le t < t_2 \\ -v_{C1} & \forall\, t_2 \le t < t_3 \\ -v_{C1} & \forall\, t_3 \le t < T_s \end{cases} \tag{9}$$

$$L_2\frac{di_{L2}}{dt} = \begin{cases} -v_{C2} & \forall\, t_0 \le t < t_1 \\ \frac{1}{L_r}E + \left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)v_{C1} + \left(\frac{L_1}{L_rL_2}-1\right)v_{C2} & \forall\, t_1 \le t < t_2 \\ -v_{C2} & \forall\, t_2 \le t < t_3 \\ -v_{C2} & \forall\, t_3 \le t < T_s \end{cases} \tag{10}$$

$$C_1 \frac{dv_{C1}}{dt} = \begin{cases} -i_{LD} & \forall\, t_0 \le t < t_1 \\ i_{L1} - i_{L2} & \forall\, t_1 \le t < t_2 \\ i_{L1} & \forall\, t_2 \le t < t_3 \\ i_{L1} & \forall\, t_3 \le t < T_s \end{cases} \tag{11}$$

$$C_2 \frac{dv_{C2}}{dt} = i_{L2} - \frac{v_{C2}}{R} \qquad \forall\, t_0 \le t < T_s \tag{12}$$

Assuming that, both the input voltage and the capacitor voltages are constant in a switching cycle, and using equations (2) and (6) through (8) according to Figure 3, the response of the inductor L_D current over a switching cycle is obtained as:

$$i_{LD} = \frac{1}{L_D} \begin{cases} v_{C1} t & \forall\, t_0 \le t < t_1 \\ i_{LD0} - \left(\frac{1}{L_r} E - \left(\frac{1}{L_r} + \frac{L_1}{L_r L_2} \right) v_{C1} + \frac{L_1}{L_r L_2} v_{C2} \right) t & \forall\, t_1 \le t < t_2 \\ i_{LD1} - E\, t & \forall\, t_2 \le t < t_3 \\ 0 & \forall\, t_3 \le t < T_s \end{cases} \tag{13}$$

Where: $i_{LD0} = v_{C1} d_1 T_s$,

$$i_{LD1} = v_{C1} d_1 T_s - \left(\frac{1}{L_r} E - \left(\frac{1}{L_r} + \frac{L_1}{L_r L_2} \right) v_{C1} + \frac{L_1}{L_r L_2} v_{C2} \right) d_2 T_s$$

$$i_{LD1} = E d_3 T_s$$

It should be noticed that d_1 is the period of time between t_0 and t_1 divided by the switching period (T_s), and in a similar way, d_2 and d_3 are the corresponding stage of time divided by the switching period. The addition of d_1 plus d_2 is the actual duty cycle of the main switch; however, d_2 is the duty cycle seen by the output stage.

Considering (9) through (12), and substituting (13), the averaging over a switching cycle is obtained as:

$$\begin{aligned} L_1 \frac{d\,\tilde{i}_{L1}}{dt} = {} & \frac{1}{T_s} \int_0^{d_1 T_s} \tilde{E}\, dt + \\ & \frac{1}{T_s} \int_0^{d_2 T_s} \left(\left(1 - \frac{1}{L_r} \right) \tilde{E} - \left(1 - \frac{1}{L_r} - \frac{L_1}{L_r L_2} \right) \tilde{v}_{C1} - \frac{L_1}{L_r L_2} \tilde{v}_{C2} \right) dt + \\ & \frac{1}{T_s} \int_0^{(1-d_1-d_2)T_s} -\tilde{v}_{C1}\, dt \end{aligned} \tag{14}$$

$$L_2\frac{d\,\tilde{i}_{L2}}{dt}=\frac{1}{T_s}\int_0^{d_1T_s}-\tilde{v}_{c2}\,dt+\frac{1}{T_s}\int_0^{d_2T_s}\left(\frac{1}{L_r}\tilde{E}+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}+\left(\frac{L_1}{L_rL_2}-1\right)\tilde{v}_{C2}\right)dt+\frac{1}{T_s}\int_0^{(1-d_1-d_2)T_s}-\tilde{v}_{C2}\,dt \tag{15}$$

$$C_1\frac{d\,\tilde{v}_{C1}}{dt}=\frac{1}{T_s}\int_0^{d_1T_s}-\frac{\tilde{v}_{C1}\mathrm{t}}{L_D}\,dt+\frac{1}{T_s}\int_0^{d_2T_s}(\tilde{i}_{L1}-\tilde{i}_{L2})\,dt+\frac{1}{T_s}\int_0^{(1-d_1-d_2)T_s}\tilde{i}_{L1}\,dt \tag{16}$$

$$C_2\frac{d\,\tilde{v}_{C2}}{dt}=\frac{1}{T_s}\int_0^{T_s}\left(\tilde{i}_{L2}-\frac{\tilde{v}_{C2}}{R}\right)dt \tag{17}$$

Then simplifying equations (14) through (17), and knowing that $d=d_1+d_2$ is obtained the next equation system:

$$\begin{aligned}
L_1\frac{d\,\tilde{i}_{L1}}{dt}&=\tilde{E}(d-d_2)-\tilde{v}_{C1}(1-d)+\left(\left(1-\frac{1}{L_r}\right)\tilde{E}-\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}-\frac{L_1}{L_rL_2}\tilde{v}_{C2}\right)d_2\\
L_2\frac{d\,\tilde{i}_{L2}}{dt}&=\left(\frac{1}{L_r}\tilde{E}+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}+\left(\frac{L_1}{L_rL_2}-1\right)\tilde{v}_{C2}\right)d_2+-\tilde{v}_{C2}(1-d_2)\\
C_1\frac{d\,\tilde{v}_{C1}}{dt}&=-\frac{1}{2f_sL_D}\tilde{v}_{C1}(d-d_2)^2+(\tilde{i}_{L1}-\tilde{i}_{L2})d_2+\tilde{i}_{L1}(1-d)\\
C_2\frac{d\,\tilde{v}_{C2}}{dt}&=\tilde{i}_{L2}-\frac{\tilde{v}_{C2}}{R}
\end{aligned} \tag{18}$$

During d_2T_s the equation (4) is valid, so that, making the average during this time is obtained:

$$\frac{1}{T_s}\int_0^{d_2T_s}\tilde{i}_{L1}\,dt+\frac{1}{T_s}\int_0^{d_2T_s}i_{LD}\,dt-\frac{1}{T_s}\int_0^{d_2T_s}\tilde{i}_{L2}\,dt=0 \tag{19}$$

Where: $i_{LD}=\frac{\tilde{v}_{C1}d_1T_s}{L_D}-\frac{1}{L_D}\left(\frac{1}{L_r}\tilde{E}-\left(\frac{1}{L_r}+\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}+\frac{L_1}{L_rL_2}\tilde{v}_{C2}\right)\mathrm{t}$

Solving and simplifying (19) is obtained:

$$\begin{aligned}&\tilde{i}_{L1}d_2-\tilde{i}_{L2}d_2+\frac{\tilde{v}_{C1}d_1}{f_sL_D}d_2+\\&-\frac{1}{2f_sL_D}\left(\frac{1}{L_r}\tilde{E}-\left(\frac{1}{L_r}+\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}+\frac{L_1}{L_rL_2}\tilde{v}_{C2}\right)d_2^2=0\end{aligned}\tag{20}$$

Solving for d_2, and knowing that $d=d_1+d_2$ is obtained:

$$d_2=\frac{\tilde{i}_{L1}-\tilde{i}_{L2}+\frac{\tilde{v}_{C1}d}{f_sL_D}}{r+\frac{\tilde{v}_{C1}}{f_sL_D}}\tag{21}$$

Where: $r=\frac{1}{2f_sL_D}\left(\frac{1}{L_r}\tilde{E}-\left(\frac{1}{L_r}+\frac{L_1}{L_rL_2}\right)\tilde{v}_{C1}+\frac{L_1}{L_rL_2}\tilde{v}_{C2}\right)$

The average model of the system is determined by (18) and (21).

2.3. Function gain of the converter

The steady state analysis for the converter is made by considering the average model, which assumes the operating point of the system, and then the system (18) is equalized to zero; that is:

$$\begin{aligned}0&=ED-V_{C1}(1-D)-\left(\frac{1}{L_r}E+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)V_{C1}+\frac{L_1}{L_rL_2}V_{C2}\right)D_2\\0&=\left(\frac{1}{L_r}E+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)V_{C1}+\left(\frac{L_1}{L_rL_2}\right)V_{C2}\right)D_2-V_{C2}\\0&=-\frac{1}{2f_sL_D}V_{C1}(D-D_2)^2+(I_{L1}-I_{L2})D_2+I_{L1}(1-D)\\0&=I_{L2}-\frac{V_{C2}}{R}\end{aligned}\tag{22}$$

From (20) is obtained that:

$$I_{L1}-I_{L2}+\frac{V_{C1}}{f_sL_D}D-\frac{V_{C1}}{2f_sL_D}D_2-\frac{1}{2f_sL_D}\left(\frac{1}{L_r}E+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)V_{C1}+\frac{L_1}{L_rL_2}V_{C2}\right)D_2=0\tag{23}$$

The operating point may be obtained from (22) and (23), and it is obtained:

$$\begin{aligned}0&=ED-V_{C1}(1-D)-V_{C2}\\0&=\left(\frac{1}{L_r}E+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)V_{C1}+\frac{L_1}{L_rL_2}V_{C2}\right)D_2-V_{C2}\\0&=-\frac{1}{2f_sL_D}V_{C1}(D-D_2)^2-\frac{V_{C2}}{R}D_2+I_{L1}(1-D+D_2)\\0&=I_{L1}-\frac{V_{C2}}{R}+\frac{V_{C1}}{f_sL_D}D-\frac{V_{C1}}{2f_sL_D}D_2-\frac{V_{C2}}{2f_sL_D}\\0&=I_{L2}-\frac{V_{C2}}{R}\end{aligned}\tag{24}$$

After algebraic manipulation is obtained:

$$
\begin{aligned}
V_{C2} &= \sqrt[3]{\mathrm{P}+\sqrt{Q^3+P^2}}+\sqrt[3]{\mathrm{P}-\sqrt{Q^3+P^2}}-\frac{a_1}{3} \\
D_2 &= \frac{V_{C2}}{\left(\frac{1}{L_r}E+\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right)\frac{ED-V_{C2}}{(1-D)}+\frac{L_1}{L_rL_2}V_{C2}\right)} \\
I_{L1} &= \frac{V_{C2}}{R}-\frac{ED-V_{C2}}{(1-D)}\frac{1}{f_sL_D}D+\frac{ED-V_{C2}}{(1-D)}\frac{1}{2f_sL_D}D_2+\frac{V_{C2}}{2f_sL_D} \\
V_{C1} &= \frac{ED-V_{C2}}{(1-D)} \\
I_{L2} &= \frac{V_{C2}}{R}
\end{aligned}
\tag{25}
$$

where: $\mathrm{P}=\frac{3a_2-a_1^2}{9}$, $Q=\frac{9a_1a_2-27a_3-2a_1^3}{54}$,

a_1, a_2, a_3 are the coefficients of a polynomial

Expression (25) involves the solution of a third order polynomial equation for V_{C2}, which is written next:

$$V_{C2}^3+a_1V_{C2}^2+a_2V_{C2}+a_3=0 \tag{26}$$

where:

$$a_1=-\frac{\left(ZEDN^2+2MNZ+ZY+ZEDX+\left(\frac{E}{L_r}T+\frac{SED}{(1-D)}T+\frac{WS}{(1-D)}-\frac{WL_1}{L_rL_2}\right)X+\left(\frac{TSY}{(1-D)}-\frac{TYL_1}{L_rL_2}\right)+\left(\frac{E}{RL_r}+\frac{SED}{(1-D)R}\right)\right)}{\left(N^2Z+ZX+\left(\frac{TS}{(1-D)}-\frac{TL_1}{L_rL_2}\right)X+\left(\frac{S}{(1-D)R}-\frac{L_1}{L_rL_2R}\right)\right)},$$

$$a_2=\frac{\left(2ZEDMN+M^2Z+ZEDY+\left(\frac{WE}{L_r}+\frac{SEDW}{(1-D)}\right)X+\left(\frac{EY}{L_r}T+\frac{SEDY}{(1-D)}T+\frac{WSY}{(1-D)}-\frac{WYL_1}{L_rL_2}\right)\right)}{\left(N^2Z+ZX+\left(\frac{TS}{(1-D)}-\frac{TL_1}{L_rL_2}\right)X+\left(\frac{S}{(1-D)R}-\frac{L_1}{L_rL_2R}\right)\right)},$$

$$a_3=-\frac{ZEDM^2+\frac{WEY}{L_r}+\frac{SEDWY}{(1-D)}}{\left(N^2Z+ZX+\left(\frac{TS}{(1-D)}-\frac{TL_1}{L_rL_2}\right)X+\left(\frac{S}{(1-D)R}-\frac{L_1}{L_rL_2R}\right)\right)},$$

$$M=\left(\frac{D}{L_r}E+S\frac{ED^2}{(1-D)}\right),\quad N=\left(\frac{SD}{(1-D)}+\frac{DL_1}{L_rL_2}+1\right)$$

$$Y=\left(\frac{(1-D)}{L_r}E+SED\right),\quad X=\left(S-\frac{L_1(1-D)}{L_rL_2}-1\right),\quad Z=\frac{1}{(1-D)}\frac{1}{2f_sL_D}$$

$$S=\left(1-\frac{1}{L_r}-\frac{L_1}{L_rL_2}\right),\quad T=\left(\frac{1}{2f_sL_D}+\frac{1}{R}+\frac{D}{f_sL_D(1-D)}\right),\quad W=\frac{ED^2}{(1-D)f_sL_D}$$

3. Performance of the proposed converter

The proposed converter offers a high step-down conversion ratio with wide duty ratio, as it will be illustrated in this section. Adding the delayed inductor L_D allow us to obtain a very low output voltage with a bigger duty cycle.

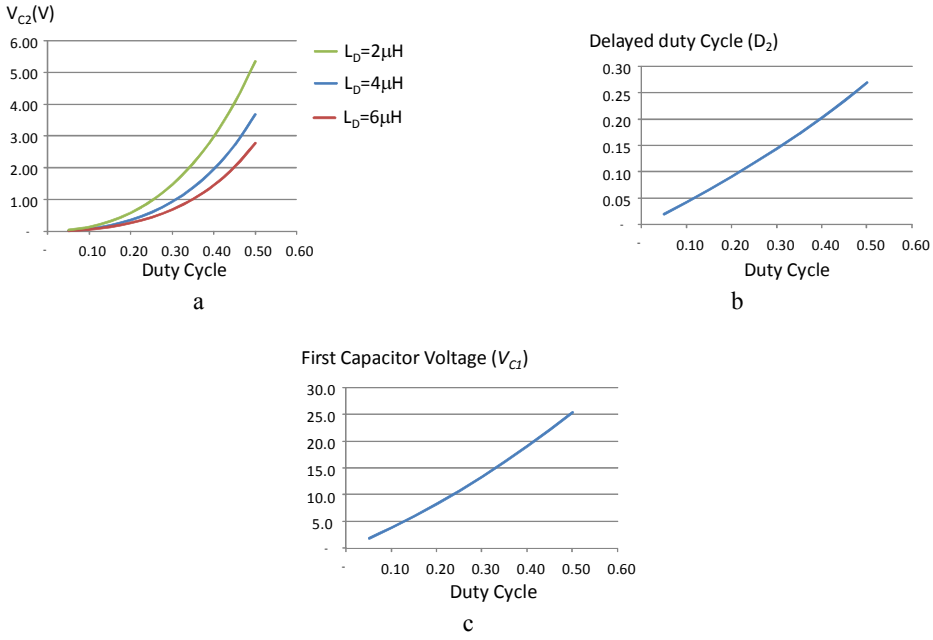


Fig. 5. *Performance of the proposed converter (DQBC)*
a Output voltage vs. duty cycle for different values of L_D
b Delayed duty cycle evolution
c Behaviour of the Capacitor V_{C1}

The converter behavior is established through equation (25), obtained in section II.C. Next parameters were considered: input voltage E of 36 V, output resistance of 0.1 Ω, switching frequency of 100 kHz at room temperature, L_1 of 150 µH, L_2 of 5 µH, C_1 of 308 µF, and C_2 of 3760µF.

The output voltage of the converter including variations of the duty cycle is illustrated in Figure 5.a, which also shows different values for the inductor L_D. As it may easily be seen, as L_D increases, a bigger duty cycle is required for the same output voltage.

The evolution for the delayed duty cycle D_2 is illustrated in Figure 5.b, where the duty cycle variations are also considered; the delayed inductor L_D is maintained constant in 2 µH for this particular case. As easily may be seen it, the duty cycle during the second stage is always lower than the actual one

The behavior of the first capacitor voltage V_{C1} is illustrated in Figure 5.c, where the variations of the duty cycle are considered; for this case the delayed inductor L_D is also maintained in 2 µH.

A comparison between the proposed converter (with L_D = 2 µH) and the traditional QBC is illustrated in Figure 6.a and 6.c. The obtained output voltage is sketched in Fig. 6.a with variations of the duty cycle. It may easily be seen that the proposed converter offers a lower output voltage for the same duty cycle. When condition V_{C2} is equal to 1.5 V, the duty cycle for the traditional QBC is around 20%, and for the proposed converter is around of 30% by using L_D equal 2µH; it is clear that a wider duty cycle is obtained

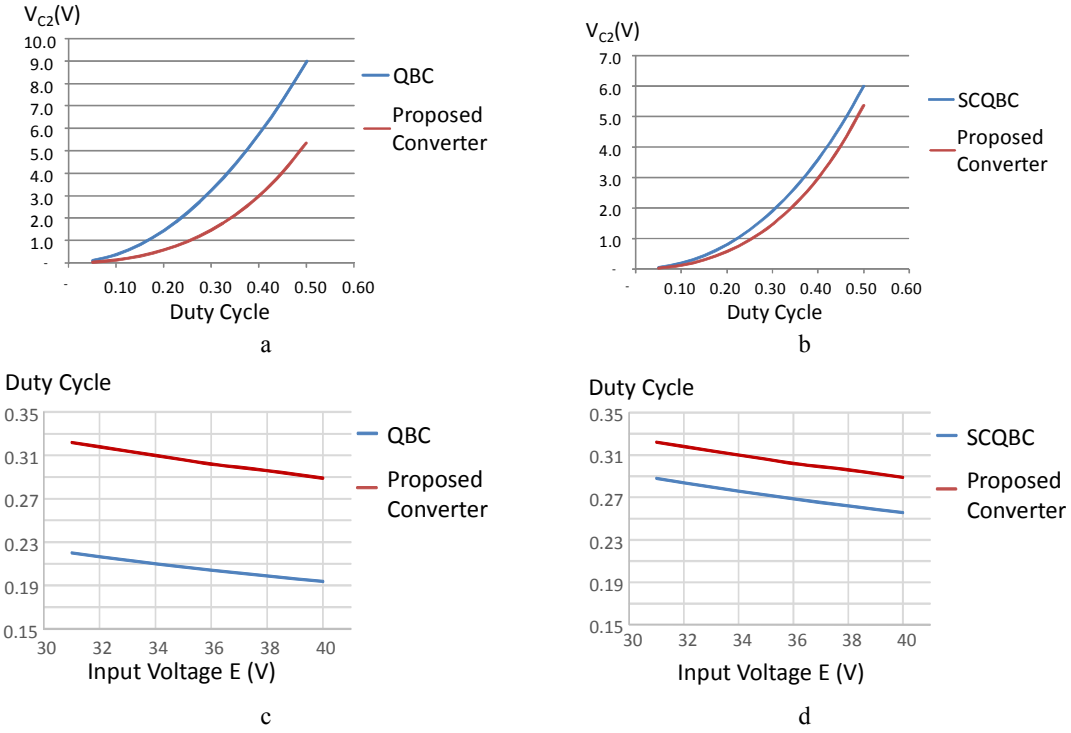


Fig. 6. *Comparison of the proposed converter (L_D=2μH) with:*
a The QBC under constant input voltage (E=36V)
b The SCQBC under constant input voltage (E=36V)
c The QBC under constant output voltage (V_{C2}=1.5V)
d The SCQBC under constant output voltage (V_{C2}=1.5V)

with the same operating conditions. However, it is important to notice that even a higher duty cycle may be obtained if L_D is increased. The obtained duty cycle is graphed with variations of the input voltage, but maintaining constant the output; as it can be observed the proposal offers a duty cycle always higher and around of 10%.

A comparison with a switched capacitor quadratic buck converter (SCQBC) [18] is illustrated in Figure 6.b and 6.d. Although this converter offers a higher duty cycle for the same output voltage, not only much more components are required, but also, the desired duty cycle cannot be selected as easily as increasing one component on this proposal. Particularly for this case, this proposal offers a wider duty cycle by simple using L_D.

A comparison for the proposed converter with the traditional QBC, and the SCQBC [18] is shown in table I. The converter, which is able to offer a very high-step-down dc-dc conversion with an important increment of the duty cycle, is the proposed converter, the SCQBC scheme also offers the possibility of achieving a high-step-down, however, many components are required. It is easily seen that the converters

Table 1 Comparison of the converter

Characteristic	Traditional QBC Converter	SCQBC [18]	Proposed Converter
Converter gain	$\frac{Vo}{Vin} = D^2$	$\frac{Vo}{Vin} = \frac{D^2}{2-D}$	Equation (25)
Active switches	1	1	1
Diodes	3	6	3
Inductors	2	2	3
Capacitors	2	3	2
Max MOSFET voltage	$Vin + V_{C1}$	$Vin + 2V_{C1}$	$Vin + V_{C1}$
Max diode current	I_o	I_o	I_o
Analysis	Simple	Simple	Complex
Step-down-conversion	Medium	Medium-High	High

Table 2 Converter characteristics

Input voltage	36V ±10%	L_1	150μH
Output voltage	1.5V	L_2	5μH
Designed output power	20W	L_D	2μH
Maximum output current	20A	C_1	308μF
Switching frequency	100kHz	C_2	3760μF
Output voltage ripple	0.05% Nominal voltage	MOSFET	IRFH5006PbF
Inductor current ripple	20% Nominal current	Diodes	MBRB3030CTL-D

with more components is the SCQBC.

The proposed converter is suitable for high-step-down conversion with reasonable duty cycles by just adding a small inductor, no complex design; however, it is complex to analyze compared to some other schemes, but also the efficiency may be penalized since more than two components conduct at the same time.

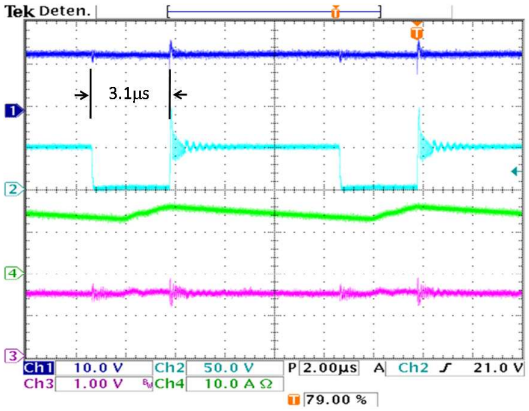
4. Experimental results

The delayed quadratic buck converter was designed and tested in the laboratory under the following operating conditions: input voltage E of 36 V, output voltage of 1.5 V, an output power of 20 W, and switching frequency of 100 kHz at room temperature. The MOSFET used is IRFH5006PbF and the diodes MBRB3030CTL-D. Once the converter was designed its resulting parameters were: L_1 of 150 μH, L_2 of 5

μH, C_1 of 308 μF, C_2 of 3760μF, and the delayed inductor L_D is 2 μH; more details see Table 2.

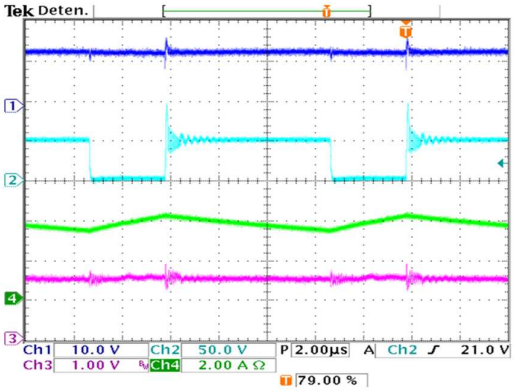
Both converters, the proposed one, and the conventional QBC were tested during operation at full load, as shown in Figure 7. For comparison purposes, the same active devices and gate driver circuits were used in both converters. The first capacitor voltage V_{C1}, voltage V_{DS} for the MOSFET, output inductor current I_{L2}, output inductor current I_{L1}, and output voltage V_{C2} are shown.

The results for the proposed converter are shown in Figure 7.a and 7.b. It is easily seen in Figure 7.a that, when the main switch is turned 'on' (zero voltage), the output inductor current is still decreasing (inductor discharge), this is explained because the voltage applied to the second stage is delayed due to inductor L_D. It is worth to mention the fact that the obtained duty ratio in the proposed converter is higher



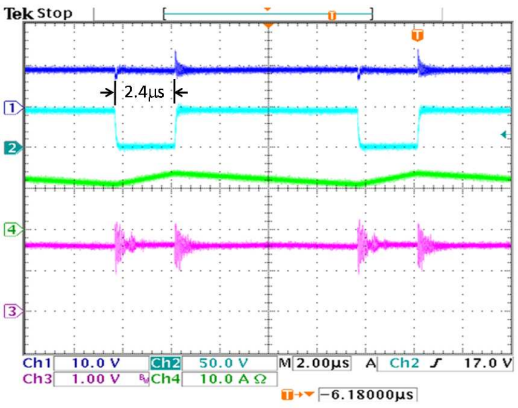
a

From top to bottom: Capacitor voltage V_{C1}, V_{DS} of the MOSFET, Output inductor Current I_{L2}, and Output voltage V_{C2}



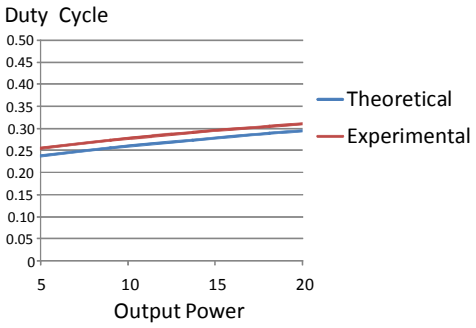
b

From top to bottom: Capacitor voltage V_{C1}, V_{DS} of the MOSFET, Input inductor Current I_{L1}, and Output voltage V_{C2}



c

From top to bottom: Capacitor voltage V_{C1}, V_{DS} of the MOSFET, Output inductor Current I_{L2}, and Output voltage V_{C2}



d

Fig. 7. *Experimental results: a) and b) Proposed DQBC, c) Traditional QBC, d) Validation*
a Proposed DQBC: Test 1
b Proposed DQBC: Test 2
c Traditional QBC
d Output voltage vs duty cycle: ideal and experimentally

than the conventional quadratic buck converter under the same conditions, as is illustrated in Figure 7.c. Therefore, the extra inductor effectively permits a wider conversion ratio for a lower output voltage.

It should be noticed that a ringing effect appears when the main switch is turned-OFF for the proposed converter, this is due to the added inductor which acts as a parasitic element at the transition. This ringing should be taken into account because it would affect adversely to the converter.

Almost the same waveforms are illustrated in Figure 7.b, with the only difference that the input inductor current is graphed instead of the output current. It may easily be seen, that this current is more similar in operation to the traditional converter, because the charge and discharge conditions agree with the main switch.

The duty cycle versus the output power is shown in Figure 7.d, but maintaining the input and output voltage constant. Experimental and theoretical results are also illustrated, it is easily seen a good agreement among them. The difference between the two graphs is due to the losses of the converter in the prototype.

The proposed converter offers a wider conversion ratio for lower output voltages as the theoretical analysis and experimental results demonstrate, and just a single inductor was added.

5. Conclusion

A delayed quadratic buck converter is proposed in this paper. This converter is based on the conventional quadratic buck converter, just an additional small inductor is considered. This allows a very high step-down conversion with a wider conversion ratio.

A comparison is made between the proposed converter with the conventional quadratic one and some recent schemes reported in the literature; clearly this proposal has the advantageous feature of having a duty ratio, which may effectively be extended easily. Analysis and equations are given with the corresponding model for the converter.

Experimental results show that the proposed converter, not only, develops a good performance, but also, are in a good agreement with the theoretical analysis.

6. References

[1] Panov, Y., Javanovic M. M.: 'Design and performance evaluation of low voltage/high current dc/dc on board modules', *IEEE Trans. Power Electron.,*2001, **16**, (1), pp. 26 – 33

[2] Zhou, X., Xu, P., Lee, F. C.: 'A novel current-sharing control technique for low-voltage high-current voltage regulator module applications', *IEEE Trans. Power Electron.,* 2000, **15,** (6), pp. 1153–1162

[3] Panov, Y., Javanovic, M. M.: 'Design Consideration for 12V-1.5V; 50 A, Voltage Regulator Modules', *IEEE*

Trans. Power Electron. 2001, **16,** (6), pp. 776 – 783.

[4] Loera-Palomo, R., Morales-Saldaña, J.A., Palacios-Hernández, E.: 'Quadratic step-down dc–dc converters based on reduced redundant power processing approach', *IET Power Electron.* 2012, **6,** (1), pp. 136–145.

[5] Wijeratne, D.S., Moschopoulos, G.: 'Quadratic Power Conversion for Power Electronics: Principles and Circuits', *IEEE Trans. on Circuits and Systems—I: Regular Papers*, 2012, **59,** (2), pp. 426–438.

[6] Pan, C., Chuang, C., Chu, C.: 'A Novel Transformer-less Interleaved High Step-down Conversion Ratio DC-DC Converter with Low Switch Voltage Stress', *IEEE Trans. Ind. Electron.*, **61,** (10), pp. 5290-5299.

[7] Lica, S., Gurbina, M., Draghici, D., Iancu, D., Lascu, D.: 'A new quadratic buck converter', *IEEE 11th International Symposium on Electronics and Telecommunications (ISETC)*, Timisoara, November 2014, pp. 1-4.

[8] Sabzali, A. J., Ismail, E. H., Al-Saffar, M. A., Behbehani, H. M.: 'Non-isolated single-switch DC–DC converters with extended duty cycle for high step-down voltage applications', *International Journal of Circuit Theory and Applications*, 2014, **43,** (8), pp. 1080-1094.

[9] Sung-Sae, L.: 'Step-down converter with efficient ZVS operation with load variation', *IEEE Trans. Ind. Electron.*, 2014, **61,** (1), pp. 591–597.

[10] Larico, H.R.E., Barbi, I.: 'Three-phase push–pull dc–dc converter: Analysis, design, experimentation', *IEEE Trans. Ind. Electron.*, 2012, **59,** (12), pp. 4629–4636.

[11] Pahlevaninezhad, M., Drobnik, J., Jain, P. K., Bakhshai, A.: 'A load adaptive control approach for a zero-voltage-switching dc/dc converter used for electric vehicles', *IEEE Trans. Ind. Electron.*, 2012, **59,** (2), pp. 920–933

[12] Moo, C. S., Chen, Y. J., Cheng, H. L., Hsieh, Y. C.: 'Twin-buck converter with zero-voltage-transition', *IEEE Trans. Ind. Electron.*, 2011, **58,** (6), pp. 2366–2371

[13] Zhu,Y., Lehman, B.: 'Control loop design for two-stage converters with low voltage/high current output', *IEEE Trans. Power Electron.,*2005, **20,** (1). pp. 44 – 55.

[14] Zhu, Y., Lehman, B.: 'Three-level switching cell for low voltage/ high current dc-dc converters', *IEEE Trans. Power Eectron.,*2007, **22,** (5), pp.1977 – 2007.

[15] Zhou, X., Wong, P.L., Xu, P. LeeF. C.: 'Investigation of Candidate VRM Topologies for Future Microprocessors', *IEEE Trans. Power Electron*., 2000, **15,** (6), pp. 1172 – 1182.

[16] Morales-Saldaña, J.A., Carbajal-Gutierrez, E. E., Leyva-Ramos, J.: 'Modeling of switch-mode DC-DC cascade converters', *IEEE Trans. Aerosp. Electron.Syst.,*2002, **38,** (1), pp. 295–299.

[17] Ortiz-Lopez, M. G., Leyva-Ramos, J., Morales-Saldaña, J. A., Carbajal-Gutierrez, E. E.: 'Modeling and Analysis of Switch-Mode Cascade Converters with a Single Active Switch', *IET Power Electron*., 2008, **1,** (4), pp. 478 – 487.

[18] Reyes, J., Vázquez, N., Leyva, J.: 'Switched-Capacitor Quadratic Buck Converter for Wider Conversion Ratios', *IET Power Electron.*, 2015, **8,** (12), pp. 2370-2376.

[19] Yeu-Torng Y., Wen-Zhuang J., Kuo-Ing H.: 'Step-Down Converter with Wide Voltage Conversion Ratio', *IET Power Electron.*, 2015, **8,** (11), pp. 2136-2144

[20] Miftakhutdinov, R., Zbib, J.: 'Synchronous buck converter with increased efficiency', *Appl. Power Electron. Conf., APEC 2007- Twenty Second Annual*, Anaheim, CA, February 2007, pp.714 – 718.

[21] Castilla, M., Garcia de Vicuña, L., Guerrero, J. M., Matas, Miret, J.: 'Design of voltage-mode hysteric controllers for synchronous buck converters supplying microprocessor loads', *IEE Proc.-Electr. Power Appl.*, 2005, **152,** (5), pp. 1171–1178.

[22] Yahaya, N. Z., Begam, K. M., Awan, M.: 'Experimental analysis of a new zero-voltage switching synchronous rectifier buck converter', *IET Power Electron.*, 2011, **4,** (7), pp. 793–798.

[23] Krein, P. T., Bentsman, J., Bass, R., Leisieutre, B.: 'On the use of the averaging for the analysis of the electronic systems', *IEEE Trans. on Power Electron.,* 1990, **5,** (2), pp 182–189.

[24] Vorperian. V.: 'Simplified Analysis of PWM Converters Using Model of PWM Switch, Part I: Continuous Conduction Mode', IEEE *Trans. on Aerosp. Electron. Syst.*, 1990, **26,** (3), pp 490–496.

[25] Dijk, E. V., Spruijt, J. N., O'Sullivan, D.M., Klassens, J. B.: 'PWM-Switch Modeling of DC-DC Converters', *IEEE Trans. Power Electron.,*1995, **10,** (6), pp. 659–665.

[26] Sun, J., Mitchell, D.M., Greuel, M.F., Krein, P.T., Bass, R.M.: 'Averaged Modeling of PWM Converters Operating in Discontinuous Conduction Mode', *IEEE Trans. Power Electron.*, 2001, **16,** (4), pp. 482-492.

[27] Morales-Saldaña, J. A., Leyva-Ramos, J., Carbajal-Gutierrez, E. E., Ortiz-Lopez, M. G.: 'Average current-Mode Control Scheme for a Quadratic Buck Converter with a Single Switch', *IEEE Trans. Power Electron.* 2008, **23**, (1), pp. 485 – 490.