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ORIGINAL RESEARCH PAPER

Switching regulator based on switched-inductor SEPIC DC-DC converter with a continuous input current for lithium-ion batteries

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Abstract

This study discusses a control strategy applied to the switched-inductor single-ended primary-inductance converter (SEPIC) converter suitable for applications where the voltage delivered by a DC source varies from above or below the nominal value. The SEPIC converter can provide a non-isolated positive output voltage for the above applications; moreover, it exhibits better characteristics when combined with a switched-inductor cell. A design-oriented procedure is given that appropriately selects the elements of the converter for a given output voltage and power delivery requirements. A control scheme with two loops is chosen. A high-gain compensator is used in the inner loop such that the average inductor current follows a current reference. A proportional integral (PI) controller is used in the outer loop for output voltage regulation. The controller was designed using loop-shaping techniques and applied to regulate an output voltage of 21 V. The design was verified with experimental results in a switching regulator where step changes were applied to the load. The performance of the switching regulator was also tested for variations of the input voltage.

1 | INTRODUCTION

There are applications in which the voltage delivered by a source varies from above or below the desired value as unregulated frequency line rectifiers, rechargeable batteries as lithium-ion, or alternative power sources like fuel cells or photovoltaic (PV) panels [1–3].

The voltage delivered by lithium-ion batteries (LIBs) varies depending on their charging status [4]. They are used in electric or hybrid vehicles as a single source or combined with fuel cells, telecommunication systems, medical equipment, or power tools. These batteries are preferred because they are lighter than other types of rechargeable batteries of the same size. Depending on the active material combined with lithium, the nominal voltage generated by an LIB is 3.6 V with a typical operating range between 3.0 and 4.2 V, or 2.4 V, with an operating range between 1.8 and 2.85 V. All-solid-state batteries have been considered as the next generation of LIBs [5]. Models for these batteries have been developed, which provide information about the electrochemical process.

Batteries based on nickel-cadmium (Ni-Cd) or nickel metal hydride (NiMH) cells are suitable for linear regulators; however, LIB packs require regulators based on DC-DC converters [6] to be used as an interface with an output load. State of health is essential for battery management, timely maintenance, and safety incident avoidance. A variety of methods for the battery state of health have been proposed [7]. LIBs experience variable load profiles with periodical frequencies up to several kilohertz caused by power electronics. In lead-acid batteries, this pattern provides benefits when they are charging. A study was conducted to analyse the influence of the frequency of ripple currents on the lifetime of LIBs [8]. This phenomenon is also studied in [9]. It is found that the increase of charge and discharge periods with a periodical frequency increases the overpotential built-up, reducing charge and discharge ability and efficiency. Additionally, the rise in root mean square (RMS) current might increase heating in the LIB, which results in a reduction of its lifetime.

A switching converter should be selected to step up or step down the output voltage of the LIB packs. The converter must

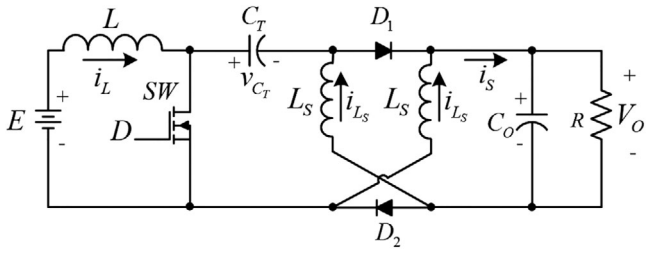


FIGURE 1 Switched-inductor single-ended primary-inductance converter (SL-SEPIC) converter

preserve the nominal value and provide smoothness to the ripple in the input and output currents to guarantee the LIB packs and load span of life.

The first option is to use a buck–boost converter, but it is not the most suitable choice because its pulsating input and output currents; then, it requires an input filter and a large output capacitor. Additionally, its output is negative with respect to the ground terminal. Another possible choice is to select an isolated flyback converter. Some of the drawbacks of this topology are its pulsating input current, a high-frequency transformer, a large switching surge due to the inductors, and the control difficulty.

If galvanic isolation is unnecessary, another possible topology to be considered is the single-ended primary-inductance converter (SEPIC), a cascade connection of boost–buck–boost converters. The removal of redundant switches avoids the arrangement's complexity and makes it relatively compact [10]. The dynamical behaviour is equivalent to a fourth-order filter; thus, it shows high robustness to noise. This converter has the same output/input voltage ratio as the buck–boost, given by D/(1-D) for a duty ratio D, except there is no polarity reversal; therefore, it can provide a lower, higher, or equal positive output voltage. It also has the feature that the metal1-oxide1-semiconductor field1-effect transistor (MOSFET) source terminal is connected to the ground, which simplifies the circuitry of the gate drive [11]. The SEPIC converter has been proposed for applications such as lighting LED lamps [12], single-phase power factor correction [13], processing energy from PV panels [14] and in unidirectional chargers, and the management of power sources of electric vehicles [15,16] among others.

Many topologies have been derived from the SEPIC converter, especially due to its non-pulsating input current. The SEPIC converter can be combined with voltage multiplier cells [17], coupled inductors [18] or both [19], switched capacitors [20], switched-coupled inductors [21], or inductor-capacitor stackable cells [22]. However, these modifications aim to obtain a high step-up voltage gain using passive elements.

Several topologies of conventional DC-DC converters with a switched inductor (SL) cell, including Cuk, Zeta, and SEPIC converters, are discussed in [23]. The combination of SEPIC with an SL cell in the output stage is shown in Figure 1. This SL-SEPIC converter presents the characteristic of step-up/step-down and input voltages with a reduced pulsating output current, which is not discussed in the original study. Only the expression for the voltage gain is given and a comparison between the total energy of the inductors magnetic field with respect to the quadratic converters, concluding that this converter uses less energy in the magnetic field, leading to savings in the inductors' size and cost.

After selecting SL-SEPIC as the converter for the switching regulator, a control strategy is required because a converter cannot regulate a voltage by itself. The controller should compensate for variations of the voltage delivered by LIB packs and the possible changes in the load. A SEPIC converter is difficult to control because of its non-minimum phase behaviour [24]; however, some interesting strategies have been proposed to control it. Sliding mode control has been proposed for charging/discharging of energy storage devices [25]. The controller uses a single sliding surface to regulate a dc-bus voltage. An indirect sliding mode controller based on the input current error only is proposed in [26]. As the SEPIC converter is a fourth-order system, a decoupling procedure is derived in [27], and then four PI controllers are designed. The resulting multiloop feedback control system can work at a broader operating condition. A controller for a PV stand-alone system is proposed in [28]. A peak-current-mode control is used with the current command generated from the input PV voltage regulating loop. Model predictive control has been proposed to control SEPIC converters with auto-tuning weighting factor capability [29].

This study aims to analyse and design a switching regulator based on the SL-SEPIC for voltage regulation of LIB packs. The steady-state operating conditions of the SL-SEPIC converter are discussed in Section 2. The expressions for the proper design of the inductors and capacitors are also given. The averaged models are derived and used to obtain the transfer functions for control purposes. In Section 3, a detailed procedure of the controller design is given, where each block's purpose is highlighted. Experimental results are shown in Section 4 to test the performance of the controller design for the converter. Final remarks are given in Section 5.

2 | MODELLING OF DYNAMICAL BEHAVIOUR OF CONVERTER

Mathematical models of a DC-DC converter should be developed to describe its dynamical behaviour. They are required in the analysis of the converter and the control strategy design to adjust the duty cycle to compensate for load and input voltage variations as well as uncertainties.

The electric diagram of the SL-SEPIC is shown in Figure 1, where V_O is the output voltage, E is the input voltage, L is the input inductor, L_S is the inductor of the cell, C_T is the capacitor that transfers energy to the output of the converter, and C_O is the output capacitor. The nominal load is denoted by R and the nominal duty cycle by D. The passive switches (diodes) are denoted by D_1 and D_2, the active switch (MOSFET) by SW, respectively. The current of input inductor is represented by i_L, the current of each SL by i_{L_S}; meanwhile, i_S is the output current of the inductor cell.

The operation of the converter is shown in Figure 2 when the active switch is turned ON or OFF. The inductors of the cell are

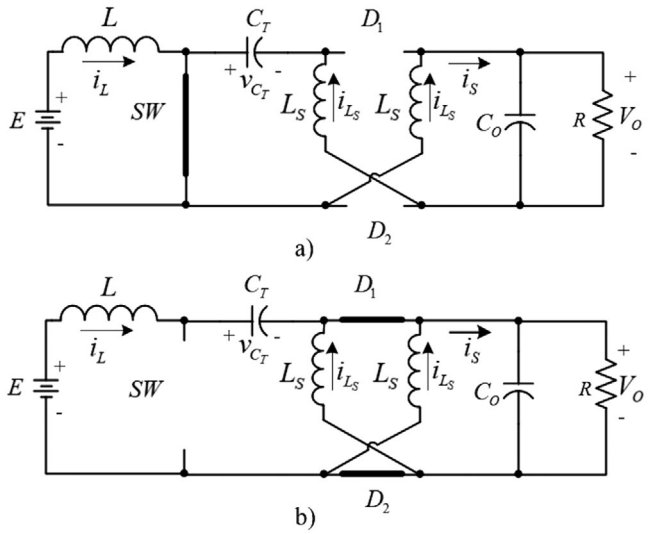


FIGURE 2 Operating modes of the SL-SEPIC converter: (a) SW is ON, and (b) SW is OFF

connected in series when the active switch *SW* is turned ON and in parallel when the active switch *SW* is turned OFF. This series-parallel connection of inductors will increase the output current, and unlike the conventional SEPIC converter, i_S continuously delivers current to the output filter.

The converter will operate in continuous conduction mode (CCM) when the currents of the inductors never decay to zero. The conditions in the inductors for the operation in CCM are:

$$L > \frac{2(1-D)^2 R}{D f_S} \quad \text{and} \quad L_S > \frac{(1-D)R}{f_S}, \tag{1}$$

where f_S is the switching frequency of the converter.

The corresponding steady-state operating conditions can be computed by

$$I_L = \frac{D^2 E}{4(1-D)^2 R}, \quad I_{L_S} = \frac{DE}{4(1-D)R},$$

$$V_{C_T} = \frac{2-D}{2(1-D)} E \quad \text{and} \quad V_O = \frac{D}{2(1-D)} E, \tag{2}$$

where V_{C_T} is the voltage of the transfer capacitor. Thus, the resulting current and voltage gains are as follows:

$$\frac{I_O}{I_L} = \frac{2(1-D)}{D} \quad \text{and} \quad \frac{V_O}{E} = \frac{D}{2(1-D)}. \tag{3}$$

As in the conventional SEPIC converter, the SL-SEPIC can provide an output voltage from above or below a nominal voltage value by adjusting the duty cycle *D*.

A converter should be designed such that the inductor currents and capacitor voltages satisfy design specifications. The ripple ratio in the inductor current is computed by $\varepsilon_{i_L} = (\Delta i_L/2)/I_L$. A value between 10% and 20% is recommended in a conventional converter. Meanwhile, the ripple ratio in the capacitor voltage is $\varepsilon_{v_C} = (\Delta v_C/2)/V_C$ with a recommended value between 1% and 2%.

The expressions for the inductors as a function of the current ripples are now given where it is assumed that the switching devices are ideal:

$$L = \frac{DE}{f_S \Delta i_L} \quad \text{and} \quad L_S = \frac{DE}{2 f_S \Delta i_{L_S}}, \tag{4}$$

and for the capacitors by

$$C_T = \frac{D^2 E}{4(1-D)R f_S \Delta v_{C_T}} \quad \text{and} \quad C_O = \frac{D^2 E}{4(1-D)R f_S \Delta v_O}. \tag{5}$$

In the converter under study, the switching inductors L_S have the same value; therefore, the current is the same in each inductor when they are connected in parallel or series. Therefore, a single variable can be used for the currents of the SLs for a fourth-order model. If the inductors are different, a peak in the inductor voltage appears when the MOSFET turns ON or OFF. These values are more significant as the difference between inductors increases.

The behaviour of the SL-SEPIC can be analysed using a linear piecewise model. A state-space representation is obtained from the operation of active switch SW depicted in Figure 2. The state variables are the first inductor current, the current of SLs, the voltage of the transfer capacitor, and the output voltage. Thus, a bilinear switching model can be obtained where i_L and i_{L_S} are the currents of first and switched inductors, v_{C_T} and v_O are the transfer capacitor voltage and output voltage, and e is the input voltage, respectively:

$$\begin{bmatrix} \dot{i}_L \\ \dot{i}_{L_S} \\ \dot{v}_{C_T} \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-q}{L} & -\frac{1-q}{L} \\ 0 & 0 & \frac{q}{2L_S} & -\frac{2-q}{2L_S} \\ \frac{1-q}{C_T} & -\frac{q}{C_T} & 0 & 0 \\ \frac{1-q}{C_O} & \frac{2-q}{C_O} & 0 & -\frac{1}{RC_O} \end{bmatrix} \begin{bmatrix} i_L \\ i_{L_S} \\ v_{C_T} \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} e \tag{6}$$

The binary switching function q has a value of 0 when the active switch SW is turned OFF and 1 when is turned ON.

Switching converters have a non-linear dynamic behaviour; however, it can be modelled by employing averaging techniques over one switching period using the state-space linear approach. Non-linear averaged models are required when it is necessary to predict converter behaviour for large variations.

Averaging techniques can be applied to obtain the corresponding average model to the state-state representation [30] where the average value of q will be denoted by $\bar{d}$; thus, the

following model is derived:

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{i}}_{L_S} \\ \dot{\bar{v}}_{C_T} \\ \dot{\bar{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-\bar{d}}{L} & -\frac{1-\bar{d}}{L} \\ 0 & 0 & \frac{\bar{d}}{2L_S} & -\frac{2-\bar{d}}{2L_S} \\ \frac{1-\bar{d}}{C_T} & -\frac{\bar{d}}{C_T} & 0 & 0 \\ \frac{1-\bar{d}}{C_O} & \frac{2-\bar{d}}{C_O} & 0 & -\frac{1}{RC_O} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{i}_{L_2} \\ \bar{v}_{C_T} \\ \bar{v}_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} \bar{e} \tag{7}$$

The system matrix depends on the average duty cycle $\bar{d}$; therefore, this model is non-linear.

The linearisation of Equation (7) around an operating point will describe its dynamic behaviour. The output voltage, input voltage, control signal, inductor currents, and capacitor voltages can be decomposed into the nominal values and the corresponding deviations. Upper-case letters denote the nominal values, whereas the deviations by the superscript ∼. Thus, the linearisation of Equation (7) results in

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{i}}_{L_S} \\ \dot{\tilde{v}}_{C_T} \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-D}{L} & -\frac{1-D}{L} \\ 0 & 0 & \frac{D}{2L_S} & -\frac{2-D}{2L_S} \\ \frac{1-D}{C_T} & -\frac{D}{C_T} & 0 & 0 \\ \frac{1-D}{C_O} & \frac{2-D}{C_O} & 0 & -\frac{1}{RC_O} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{i}_{L_S} \\ \tilde{v}_{C_T} \\ \tilde{v}_O \end{bmatrix} + \begin{bmatrix} \frac{E}{(1-D)L} \\ \frac{E}{2(1-D)L_S} \\ -\frac{DE}{4RC_T(1-D)^2} \\ -\frac{DE}{4RC_O(1-D)^2} \end{bmatrix} \tilde{d} \tag{8}$$

This model helps to analyse the converter for performance and implementation; however, it is essential to obtain the appropriate transfer functions. By applying the Laplace transform of the state-space representation given by Equation (8), the transfer function first inductor current-to-control signal is derived as

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{9}$$

where

$$a_3 = \frac{1}{RC_O},\ a_2 = \frac{(D-1)^2(C_T + C_O)}{C_T C_O L} + \frac{(D-2)^2}{2C_O L_S} + \frac{D^2}{2C_T L_S},$$

$$a_1 = \frac{1}{C_T C_O R}\left[\frac{(1-D)^2}{L} + \frac{D^2}{2L_S}\right], \quad a_0 = \frac{2(D-1)^2}{C_T C_O L L_S},$$

$$b_3 = \frac{E}{L(1-D)}, \quad b_2 = \frac{E(1+D)}{RL(1-D)}\left[\frac{1}{C_T} + \frac{1}{C_O(1+D)}\right],$$

$$b_1 = \frac{E(DL_S + 4C_T R^2 - 2C_T D R^2 + 2C_O D R^2)}{4R^2 C_T C_O L L_S (1-D)},$$

$$b_O = \frac{ED}{C_T C_O L L_S R(1-D)}.$$

Meanwhile, the transfer function of the output voltage-to-control signal can be expressed by

$$\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{c_3 s^3 + c_2 s^2 + c_1 s + c_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{10}$$

where

$$c_3 = -\frac{ED}{4C_O R(1-D)^2}, \quad c_2 = \frac{E}{C_O}\left[\frac{1}{L} + \frac{2-D}{2L_S(1-D)}\right],$$

$$c_1 = -\frac{ED^2}{4C_T C_O R L_S (D-1)^2} \quad \text{and} \quad c_0 = \frac{E}{C_T C_O L L_S}.$$

The transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ is stable and non-minimum phase, that is, it has zeros located in the right half-plane (RHP), whereas the transfer function $\tilde{i}_L(s)/\tilde{d}(s)$ is stable and minimum phase.

3 | CONTROLLER DESIGN USING LOOP-SHAPING

The SL-SEPIC has non-linear dynamic behaviour, and the controller design is more complicated using non-linear techniques. However, a controller can be designed using the linearised model derived in the previous section using linear control techniques. Additionally, the cost for the implementation of non-linear controllers is higher, and there is a greater risk of damaging the hardware if it is not carefully implemented [31]. Non-linear controllers are affordable for more sophisticated systems where there are no adequate linear approximations; thus, a linear controller is selected in this work.

Current-mode control is a widely used scheme to control switched converters. It has many advantages over voltage-mode control: (a) Easier-to-design control loop, (b) a faster transient response, and (c) overcurrent protection. For the controller's implementation and performance, an important issue is the appropriate selection of the variables used for feedback.

The use of voltage-mode control is not suitable for this converter due to a high-gain controller that may produce instability. Given that the transfer function $\tilde{i}_L(s)/\tilde{d}(s)$ of the SL-SEPIC converter is a minimum phase for typical values of the converter, it is more appropriate to use a current-mode control scheme. The input inductor current and output voltage are the variables that can be selected for current-mode control [32]. The inductor current will provide a faster transient response. Sensing inductor current can also be used for current overload

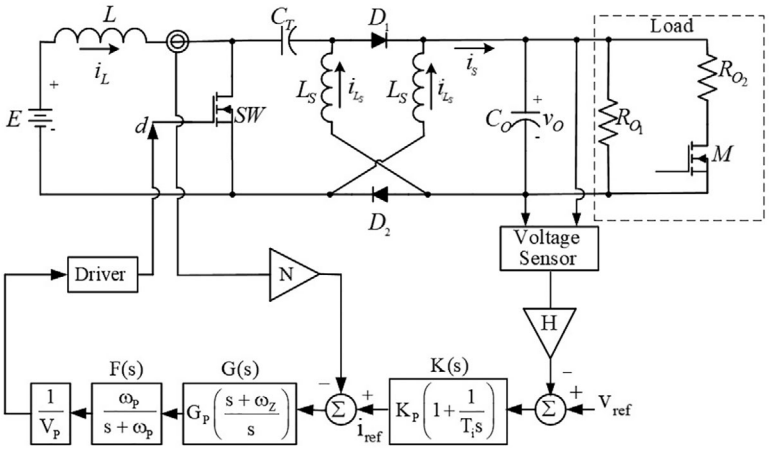


FIGURE 3 Switching regulator for an SL-SEPIC

protection through the converter. Therefore, these two feedback loops are sufficient to get a good regulation performance, even though this converter has four state variables.

An average current-mode control scheme is selected for the switching regulator (see Figure 3). The overall controller design procedure for this scheme is a twofold problem. The inner loop uses a high-gain compensator and a low-pass filter to guarantee that the average inductor current follows the current reference. The outer loop uses a PI controller for output voltage regulation. The inner loop is composed of a current sensor gain N, a high-gain compensator $G(s)$, a low-pass filter $F(s)$, and an oscillator ramp of size V_P. The voltage loop is composed of the gain H that stands for the voltage sensor, v_{ref} the desired output voltage, and $K(s)$ a *PI* controller.

Loop-shaping techniques are now used to design the controller [33]. The resulting controller gives a loop transfer function with adequate performance and stability margins when designed in the frequency domain [34]. The gain and phase at the crossover frequency are essential parameters that determine the switching regulator's robustness. One of the advantages of this method is that the resulting theoretical model, unlike other methods, can be verified experimentally by using a frequency response analyser. The procedure is easy and can be implemented with excellent results.

Closed-loop robustness is obtained when the loop gain satisfies the following conditions: (a) A high gain at low frequency, which improves the steady-state accuracy; (b) a slope of the loop gain at or near crossover frequency should be not more than –20 dB/dec, which improves the sensitivity, and (c) a loop gain with appropriate phase and gain margins for robust stability. These conditions are used to set the gain values of the controller; meanwhile, the poles and the zeros are set mainly by the operating switching frequency. The guidelines to design the controller are now given.

3.1 | Current loop

The control law for the current loop has the following form:

$$\tilde{d} = \frac{1}{V_P}\underbrace{\left(G_P\left(\frac{s+\omega_Z}{s}\right)\right)}_{G(s)}\underbrace{\left(\frac{\omega_P}{s+\omega_P}\right)}_{F(s)}(\tilde{i}_{ref} - N\tilde{i}_L), \tag{11}$$

where $G_P$is the gain, ω_Z is the location of the zero, and ω_P stands for the location of the pole. The current signal $\tilde{i}_{ref}$ is a voltage signal obtained as the output of the voltage loop used as a reference signal of the current loop, and $N\tilde{i}_L$is a voltage signal proportional to the current through the inductor detected by the current sensor. The zero ω_Z should be placed at least a decade below half of the pulse-width modulation (PWM) switching frequency [34]. The relationship that sets this value is given by $\omega_Z = 1/(R_F C_{FZ})$, where R_F is the resistance and C_{FZ} the capacitance of the high-gain compensator as shown in Figure 4.

The pole ω_P should be placed either at $f_S/2$ or above. The values of high-gain compensator are determined by the expression $\omega_P = (C_{FZ} + C_{FP})/(R_F C_{FZ} C_{FP})$where C_{FP} is the capacitor associated with the low-pass filter of the current loop.

The compensator gain is computed by the relationship $G_P = R_F/R_I$ where the resistances should be selected such that

$$G_P < \frac{20 V_p R(1-D)^3}{EDN}, \tag{12}$$

to guarantee the conditions that provide stability and good performance of the current loop.

3.2 | Voltage loop

A PI controller is designed to provide regulation to the output voltage. The reference $\tilde{i}_{ref}$is the output of this loop given by

$$\tilde{i}_{ref} = \underbrace{K_P\left(1 + 1/(T_i s)\right)}_{K(s)}(\tilde{v}_{ref} - H\tilde{v}_O), \tag{13}$$

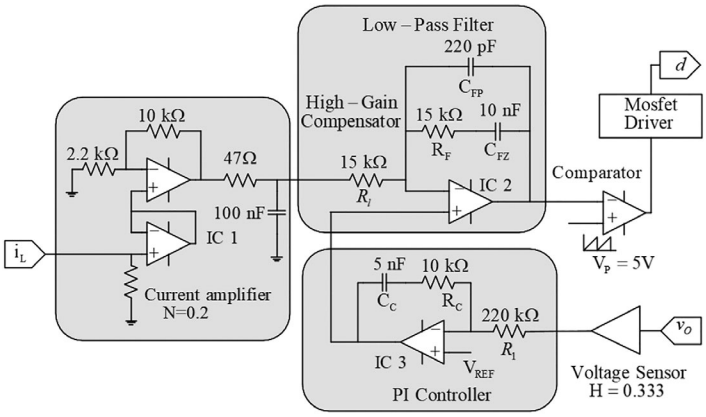
where v_{ref} is the reference for the output voltage, K_P the proportional gain, and T_i the integrative time.

The proportional gain is given by $K_P = R_C/R_1$, where the resistances have to be selected such that

$$K_P < \frac{ND}{HR(1-D)} \tag{14}$$

to achieve stability and good performance conditions for the voltage loop.

FIGURE 4 Proposed controller with two loops



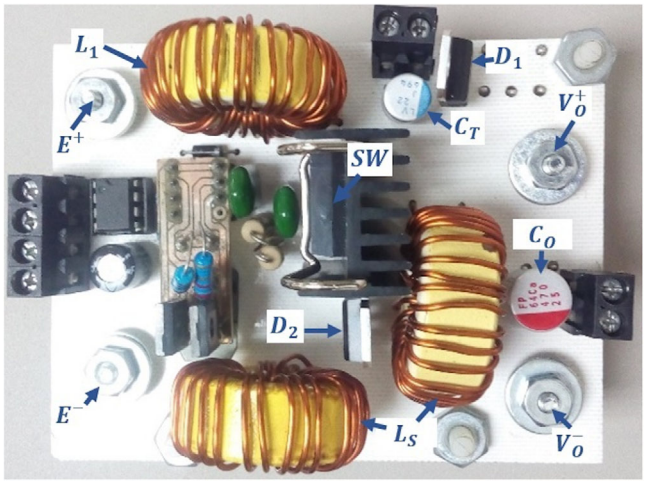


FIGURE 5 Photo of prototype

TABLE 1 Experimental prototype parameters

Parameter component	Value and information
Input voltage (E)	
Output voltage (V_O)	17.5–24.5 V
Switching Frequency (f_S)	21 V 100 kHz
Inductor (L)	Ferrite toroid, 122 μH, ESR 43 mΩ
Inductor $(L)_S$	Ferrite toroid, 81 μH, ESR 34 mΩ
Capacitor (C_O)	Aluminum organic polymer, 45 μF, 25 V, ESR 20 mΩ, RNS1E470MDN1
Capacitor (C_T)	Aluminum organic polymer, 22 μF, 63 V, ESR 35 mΩ, PLV1J220MCL1
Load (R)	3.675 Ω
Diodes	STPS60150CT, on-voltage 0.72 V
MOSFET (SW)	IRFP4468, I_D = 180 A, on-res 2.6 mΩ
MOSFET (M)	IRFP4004, I_D= 195 A, on-res 1.7 mΩ
IC 1–IC 3	TL81
Comparator	LM 311
Current sensor	LA50P, closed-loop Hall DC to 200 kHz

H is the voltage sensor gain. The integrative time is obtained by $T_i = R_C C_C$, where R_C the resistance and C_C capacitance values of the PI controller. These values should be selected such that $1/T_i$ is placed at least a decade below f_S.

4 | EXPERIMENTAL RESULTS

An SL-SEPIC converter was implemented in the laboratory. The proposed controller diagram is shown in Figure 4 and the photo of the prototype in Figure 5. The nominal values for the input and output voltages are 21 V; later variations to the input voltage are applied. These values were selected to simulate the regulation of an input voltage from an LIB pack with a nominal value that varies from 17.5 to 24.5 V. The nominal duty cycle was adjusted to $D = 0.667$, and a switching frequency of 100 kHz was selected. The resistive load was 3.675 Ω, which delivers an output power of 120 W. The theoretical steady-state operation conditions of the inductors are: $I_L = 5.73$A, and $I_{L_S} = 2.86$A, and for the capacitors $V_{C_T} = 42$V, and $V_O = 21$V.

The capacitors and inductors are designed with the following ripple ratios: $\varepsilon_{i_L} = 10\%$, $\varepsilon_{i_{L_s}} = 15\%$, $\varepsilon_{v_O} = 1\%$ and $\varepsilon_{v_{C_T}} = 1\%$. The corresponding inductor current ripples are: $\Delta i_L = 1.15$A, and $\Delta i_{L_S} = 0.86$A, and for the capacitor voltages $\Delta v_{C_T} = 0.84$V, and $\Delta v_O = 0.42$V. The parameters of the converter are listed in Table 1. The inductors were built in the laboratory, and the capacitors were adjusted to their nearest commercial value.

Using the expression for the transfer and output capacitor of the conventional SEPIC converter, they were 68 μF, which are greater than those obtained for the SL-SEPIC converter. Using the parameters of Table 1, the transfer functions of the SL-SEPIC were computed. The transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ is a fourth-order function where the poles are located at $\{(-1.97 \pm j18.61) \times 10^3, (-1.02 \pm j7.78) \times 10^3\}$, and zeros at $\{77.14 \times 10^3, (1.42 \pm j11.74) \times 10^3\}$. The transfer function $\tilde{i}_L(s)/\tilde{d}(s)$ has the same poles but the zeros are located at $\{(-1.45 \pm j18.76) \times 10^3, -6.09 \times 10^3\}$. It can be noticed that both transfer functions are stable and $\tilde{v}_O(s)/\tilde{d}(s)$ have three RHP zeros.

The current sensor gain is $N = 0.2$, and the voltage sensor gain is $H = 0.333$. The designed controller has the zero of the

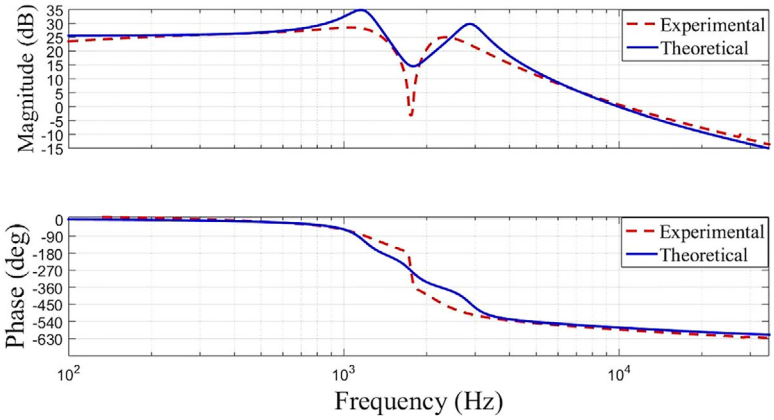


FIGURE 6 Comparison between experimental and theoretical frequency responses of transfer function output voltage-to-duty cycle: (top) magnitude (*y*-axis: 5 dB/div), and (bottom) phase (*y*-axis: 90 deg/div)

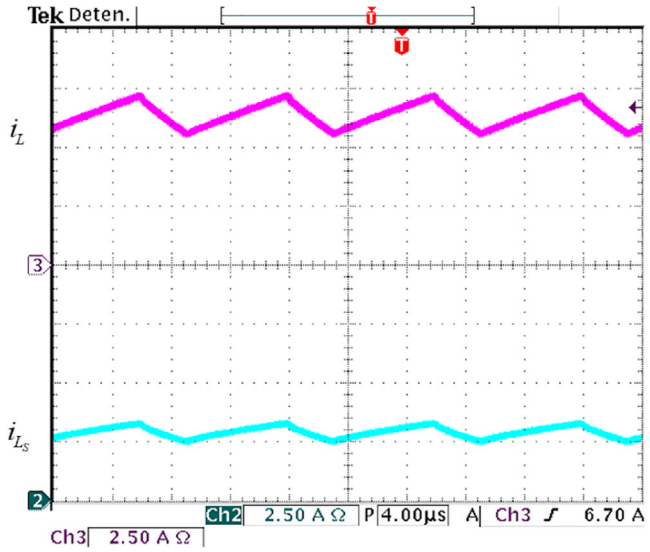


FIGURE 7 Inductor currents: (top) $i_L(t)$ (*y*-axis: 2.5 A/div), and (bottom) $i_{L_S}(t)$ (*y*-axis: 2.5 A/div) (*x*-axis: Time 4 µs/div)

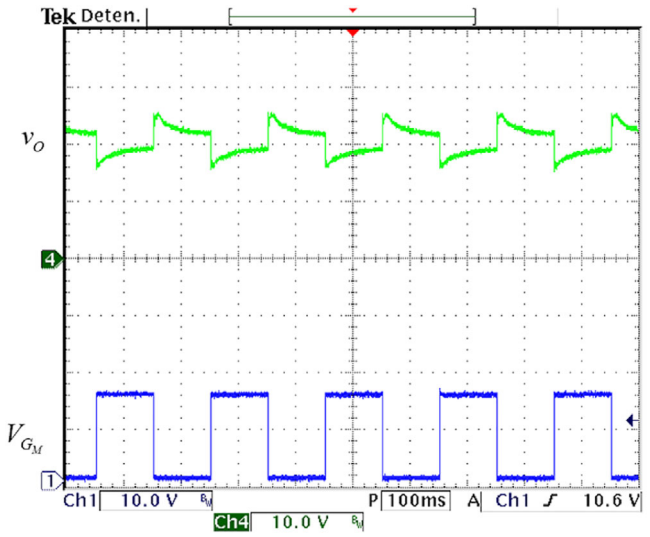


FIGURE 8 Time response in open loop to step changes in the load: Output voltage of converter v_O (*y*-axis: 10 V/div), (*x*-axis: Time 100 ms/div)

high-gain compensator located at $f_Z = 1061$ Hz, and the low-pass filter has the pole located at $f_P = 50$ kHz. The integrative time of PI controller was selected for $T_i = 50$ µs. Using the inequality given in Equation (12), the gain of the compensator should satisfy $G_P < 4.89$; therefore, this gain was selected with a value of one. Moreover, the PI-controller gain should satisfy the inequality given in Equation (14) for a value $K_P < 0.326$, where R_1 was adjusted for a value of $K_P = 0.045$. The selection of controller parameters is shown in Figure 4, where the control signal is given by

$$\tilde{d} = -60.6 \times 10^3 \times \frac{(s + 6.66 \times 10^3)}{s(s + 309 \times 10^3)} \tilde{i}_L - 4.58 \times 10^3 \times \frac{(s + 20 \times 10^3)(s + 6.66 \times 10^3)}{s^2(s + 309 \times 10^3)} \tilde{v}_O \quad (15)$$

4.1 | Open-loop test

To validate the lineal model of the SL-SEPIC converter obtained in Equation (8), the frequency responses of the theoretical and experimental transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ were compared and depicted in Figure 6.

The Frequency Response Analyser 300 from AP Instruments was used to obtain the experimental plot at nominal load. For a coherent comparison, the modulator gain $1/V_p$ was included in Equation (10). The slight differences between the theoretical and experimental results are mainly due to the parasites of switching devices and passive elements of the converter. For simplicity, these were neglected in the model.

The SL-SEPIC converter was now tested in open loop. The duty cycle of the converter was set for an output voltage of 21 V. The converter was operating in CCM as shown by the experimental inductor currents depicted in Figure 7. The average value of i_L is 6.3 A with a ripple of 1.3 A, and the average value of i_{L_S} is 2.86 A with a ripple of 0.86 A. The small differences between these values and the theoretical ones are due to losses produced by the converter's parasites.

To exhibit the behaviour of the converter in the open loop, step changes were applied to the load. This was done through the connection of an additional load at a frequency of 5 Hz as shown in Figure 3. When the MOSFET *M* is OFF, the load is

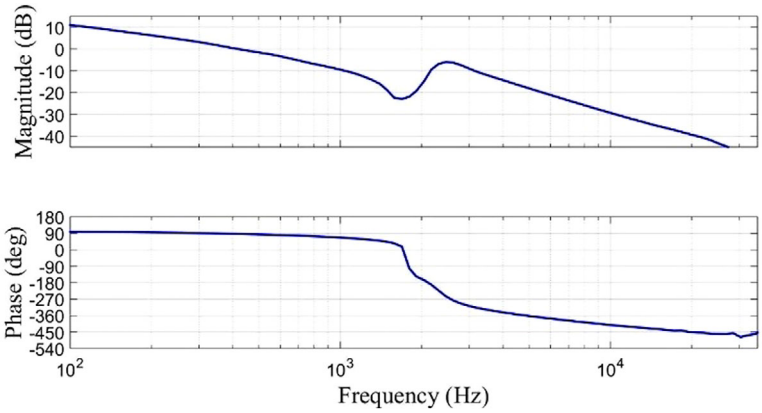


FIGURE 9 Experimental voltage loop gain at nominal load: (top) magnitude (*y*-axis: 10 dB/div), and (bottom) phase margin (*y*-axis: 90 deg/div)

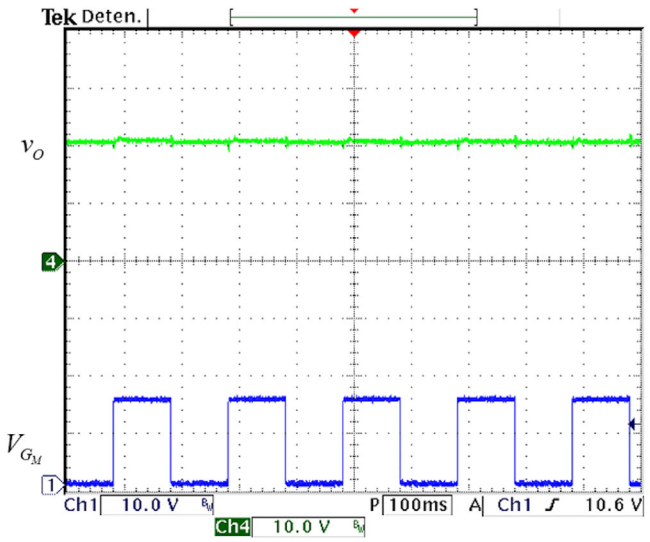


FIGURE 10 Output voltage response in closed loop to step changes in the load: (*y*-axis: 10 V/div), (*x*-axis: Time 100 ms/div)

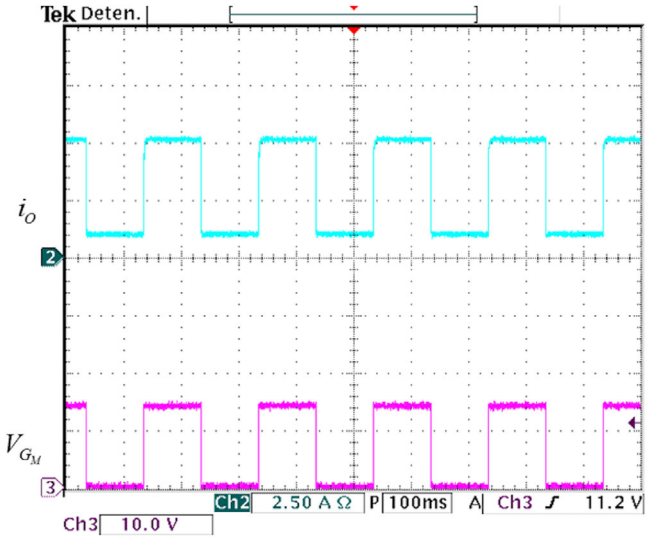


FIGURE 11 Current output response to step changes in the load: (*y*-axis: 2.5 A/div), (*x*-axis: Time 100 ms/div)

22 Ω, and when it is ON, the load is 3.675 Ω. In the first case, the demanded power is 20 W and in the second case is 120 W. The output voltage response to the load changes is depicted in Figure 8. The value of V_{G_M} is the voltage of the gate in the MOSFET *M*, so it represents the pulses when the switch is ON and OFF. As can be seen, the output voltage changes from 16 to 26 V when the changes of V_{G_M} occur. The output voltage of the converter is unregulated.

4.2 | Closed-loop test

The frequency response was obtained for the voltage loop gain and depicted in Figure 9. The PI controller dominates the loop gain at low frequencies. The voltage loop exhibits a gain margin of 6 dB and a phase margin of 86.6 degrees; robust stability is satisfied for the switching regulator.

The output voltage of the closed-loop system was set to 21 V through the duty cycle. Load changes were applied again at a frequency of 5 Hz. The demanded power changed from 20 to 120 W. The output voltage remained constant as shown in Figure 10. The current of the output is shown in Figure 11. The output current had a rapid response and did not exhibit spikes despite changes in the load.

Changes in input voltage were applied from 17.5 to 24.5 V to show the controller's behaviour for possible changes of an input voltage that varies from above or below the nominal value. As shown in Figure 12, the output voltage remained constant at 21 V despite these changes. Then, the SL-SEPIC was able to regulate the voltage variations due to LIBs.

Finally, the efficiency of the power converter was computed and depicted in Figure 13. The efficiency of the converter is defined as output power/input power. The plot was obtained connecting different load values to the prototype from 20 to 120 W and measuring the input and output powers. As can be seen, the efficiency between 60 and 120 W is above 90%. The efficiency decreases at low power because the switching devices require a small voltage to operate.

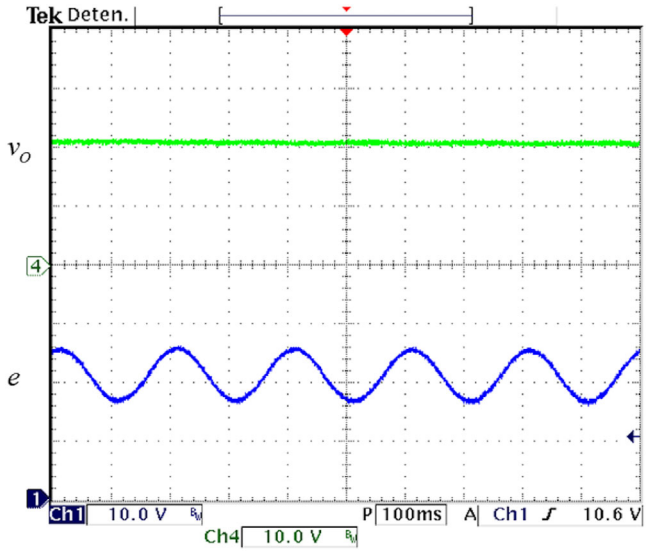


FIGURE 12 Output voltage of the switching regulator when a variable input voltage was applied: v_O (y-axis: 10 V/div), and e (y-axis: 10 V/div), (x-axis: Time 100 ms/div)

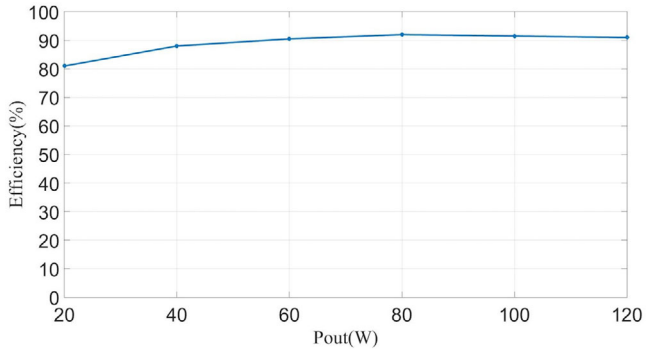


FIGURE 13 Efficiency of the SL-SEPIC converter

5 | CONCLUDING REMARKS

The conventional SEPIC converter is appropriate for applications where the power source's voltage varies from above or below the nominal value. The SEPIC converter's modified scheme in this work provides a reduced pulsating current using an SL cell in the output stage, which always delivers current to the output filter. The elements of the converter can be designed through the expressions given in this work. Moreover, it is found that the transfer and output capacitors for the SL-SEPIC converter are lower than in the conventional converter. Using linear system tools, the transfer functions inductor current-to-duty cycle and output voltage-to-duty cycle are obtained and used to implement an average current-mode controller. Even though this converter has four state variables, a reduced controller is obtained, sensing only two state variables, that is, the input current and the output voltage. Loop-shaping techniques are useful for robust controller design. A switching regulator prototype with 91% power efficiency shows good performance even for variations in the input voltage and step changes in the load. The experimental results show that the SL-SEPIC converter's designed controller performs quite well.

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