Control Scheme for a Quadratic-Based Step-Down On-Board DC/DC Converter to Be Used in Hybrid Electric Vehicles

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Abstract: This paper discusses a switching regulator with a quadratic-based step-down DC/DC converter designed using a reduced redundant power processing principle. This converter benefits from a non-complex topology, which aims to process energy more efficiently. The switching regulator can be used on-board in hybrid electric vehicles and has a non-pulsating input current, which is suitable to process energy from lithium-ion batteries. Design expressions and steady-state operating conditions are given for the converter. Models are obtained to design and implement a two-loop controller. The simplicity of this approach is of significant value in a method of design-oriented analysis, in which the analytic results can be used to make design choices. Loop-shaping techniques are used to design a robust controller to regulate the output voltage of the proposed converter under voltage variations on the lithium-ion batteries and the changes in load current requirements, as well as parameter uncertainties of the converter. The design conditions for the gains of the controller are derived. The models of the converter are verified through experimental results for a 300 W prototype and used to design a robust controller. Finally, closed-loop time and frequency domain tests are given to show the performance of the switching regulator.

Keywords: lithium-ion batteries; step-down DC/DC converter; loop-shaping control; hybrid electric vehicles

1. Introduction

In the next decades, reducing CO_2 emissions will be one of the automotive industry's main tasks, which is answered by proposing the use of low-carbon forms of energy and a stronger focus on using power more efficiently [1]. However, internal combustion engine vehicles cannot achieve these objectives, so there has been an increasing interest in hybrid electric vehicles.

A scheme of a 48 V hybrid electric vehicle system [2] is shown in Figure 1. This system includes an electrical machine, a 48 V/12 V DC/DC converter as a central component, and a 48 V battery, which helps to reduce CO_2 emissions and fuel consumption. It provides energy to the electric drive and electrical system and stores the energy from the regenerated braking. Another fundamental component is the 48 V/12 V DC/DC converter that is used to power equipment. Sensors for currents, positions, and temperatures are typically powered by a 12V [3] as well as heaters and electric pumps.

Other hybrid systems use higher voltage or so-called full hybrids or plug-in hybrids, in which a high-voltage battery (400 V nominal or up) is charged externally [4]. The on-board battery charger consists of either a single-stage converter or two-stage converter. A distributed scheme is preferred to achieve this voltage with a DC/DC converter on-board. With this action, the use of cables with a more significant cross-section to conduct high

currents is avoided, contributing to a low weight in vehicles that is proposed as one of the target objectives in the current automotive industry.
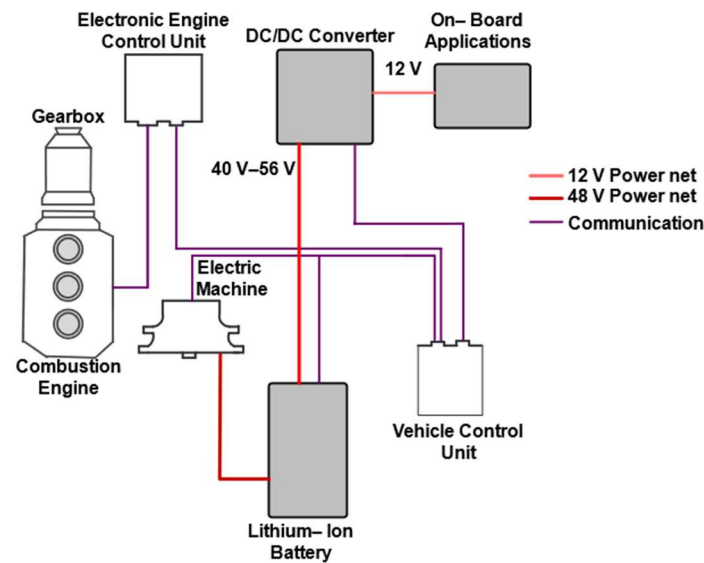

Figure 1. Hybrid 48 V/12 V system.

For the first case, only a power factor corrector (PFC) can be used to satisfy the requirements of both the supply and battery sides. For the second case, a PFC and a DC/DC converter can be used to satisfy the supply-side and the battery-side requirements, respectively [5]. Besides the battery, this system includes powerful components that allow for higher speeds and greater range in electric operation, such as an electric generator motor that propels the vehicle and works with the regenerative brake system to convert part of the braking energy into electricity. Other equipment is an inverter as an interface between the battery and electric motor, drive management, and a DC/DC converter for supplying the low-voltage to the on-board electrical system from its high-voltage counterpart.

Lithium-Ion batteries (LIB) are preferred in hybrid electric vehicles because lithium is a very reactive element [6]. In addition, the batteries have a high energy density; therefore, smaller sizes and weights are preferable to other rechargeable batteries with similar power characteristics [7]. The serial and parallel interconnection of LIBs provides arrangements with different nominal voltages and currents. A nominal 48 V of a LIB has an output voltage that varies from 40 V when the battery is discharged to 56 V when it is fully charged; thus, these batteries require a voltage regulator based on a DC/DC converter to provide proper operation. Another essential issue in a LIB is the behavior of its output current. For example, faster charge and discharge periods, high ripple currents, or high harmonic currents are detrimental to a LIB performance compared to a constant current scheme with an identical mean current [8]. Also, they increase heating and the overpotential built-up, thus negatively affecting the efficiency [9,10]. Then, the DC/DC converter that interfaces LIB to on-board applications must have a wide voltage conversion ratio and a non-pulsating input current.

A candidate topology to be considered is a conventional buck converter [11]; unfortunately, it has the drawbacks of a limited conversion ratio output-input voltage and a pulsating input current, so it is unsuitable for the proposed application. Topologies with wider conversion ratios can be found in the open literature. For example, the cascade connection of buck converters provides a lower output voltage V_O given as a function of the input voltage V_{in} by $V_O = MV_{in}$ where $M = \prod_{i=1}^{n} D_i$ is the product of D_i duty cycles of each stage. A drawback of this topology is the reduction in efficiency caused mainly by losses in the switching devices. Therefore, several topologies of two converters connected in a cascade have been proposed and operated only by a single active switch with a quadratic conversion ratio. Quadratic buck converters (QBC) can be an excellent option for

higher reduction voltage. First, the modeling is developed in [12], and later, the dynamic behavior is studied in detail for control purposes [13]; however, these topologies exhibit low efficiencies.

The efficiency of high-gain converters can be improved using non-cascaded topologies. A two-switch fifth-order DC/DC buck converter is described in [14] for a duty cycle D. A fourth-order DC/DC converter with nonlinear voltage gain is analyzed and controlled by sliding mode techniques [15]. This converter shows good switching operation, reduced voltage/current stress on components, and has a minimum phase behavior; however, its source current is pulsating. Nevertheless, both topologies have smaller conversion ratios than QBCs.

Other attempts to reach wider voltage conversion ratios without low duty cycle values have been proposed using switched-capacitor and switched-inductor-based DC/DC step-down converters [16]. The conversion ratio between input and output is widened when capacitor or inductor cells are combined with QBCs [17]; however, adding more elements increases the related losses. Another advantage of using this class of cells is that two or more can be added in the final stage. In addition, there are transitory states between ON and OFF conditions; thus, obtaining an average model to analyze the dynamic behavior is difficult.

A wide conversion range can be obtained with LCC converters which have favorable characteristics, such as high power density, and electrical isolation. However, some of the most common topologies, such as full-bridge or TL-LLC, require more complex control circuitry since they have many switching devices, and it is necessary to design dead times [18]. However, another inconvenience is their input pulsation current. Interleaved buck converters (IBC) have been proposed in [19,20] with lower switching losses and an improved conversion ratio. In ref. [21], a two-stage IBC is proposed. A buck-boost converter is used for the first and the second stage is built up by a two-phase interleaved buck converter with an active clamp and uses soft-switching techniques. Although this paper focuses on minimizing the output voltage ripple, a maximum efficiency of 89% is obtained with an output power of 192 W. However, the principal drawback of IBC is that when a small duty cycle is required, the inductor current ripples become significant, which increases the conduction losses in inductors and MOSFETs.

A regulator must be incorporated when the input voltage of the converter changes its value, but it needs to provide a constant voltage at the output. A regulator that can be used in the proposed application is the 60 V synchronous step-down switching regulator marketed by the Rohm Semiconductor company with model BD9622MUV [22], which works with input voltage ranges from 10 V to 56 V and a 12 V output for a typically handled power of 120 W and based on a hysteresis control scheme. The use proposed by the manufacturer is in entertainment machines, industrial and office automation equipment, and LED lighting. However, it is not recommended for use in equipment that requires extremely high reliability, such as medical equipment, transportation equipment, automobile equipment, or aircraft/spacecraft applications.

The reduced redundant power processing (R^2P^2) was proposed for PFCs. This principle was used for generating structures based on the non-cascaded interconnection of conventional converters for PFC to reduce losses [23]. When this principle is used, power efficiency is increased by providing a direct path to the load. The above translates into an improvement while maintaining the conversion capacity of the QBC. Several topologies based on this principle have been reported in the open literature. However, many still need to be studied in detail. For example, the quadratic-based step-down converter scheme described in [24] is shown in Figure 2, in which V_{in} represents the input voltage and V_O the output voltage. The transfer capacitor is represented by C_T and the output capacitor by C_O. The inductor of the first stage is L_1 and the inductor of the second stage is L_2. The MOSFETs M_1 and M_2 are the active switches operating simultaneously, D_1 and D_2 are the diodes, and R stands for the load.
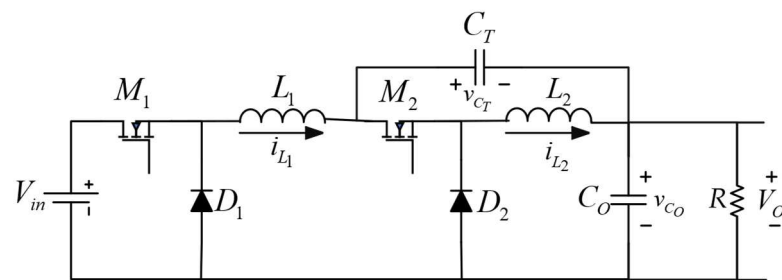
Figure 2. Electric circuit for quadratic-based step-down converter using reduced redundant power processing.

This topology has the advantage that both active switches operate with the same duty cycle, substantially facilitating the design and implementation of the MOSFET driver circuit. After the steady-state expressions and the dynamic models have been obtained, an analysis by linearization and control methods still needs to be carried out. As mentioned, one of the major problems of the conventional buck converter is the pulsating input current; this represents a drawback for many applications of power sources [25].

Another problem in these converters is the strong electromagnetic interference (EMI) due to pulsating input current and the switching action of the semiconductor devices. An LC input filter can be placed between the power source and the switching converter to preserve the integrity of the input power. However, it is well-known that adding an LC filter to the input port may cause closed-loop instability [26], leading to the need to add damping to the filter. This problem can be approached from an impedance viewpoint.

This paper aims to give general insight into the mechanisms of designing a switching regulator using a quadratic-based step-down converter combined with an input filter (QCIF) [27] and to find simple and easy-to-use expressions for the proper selection of the parameters of the converter as well of the robust controller. In practice, the stability of a mathematical model is insufficient to guarantee acceptable system performance or even to guarantee the stability of the physical system that the model represents. Therefore, there is a need to determine how far the system is from instability. This degree of stability is known as relative stability. The resulting bandwidth is determined mainly by the converter. Also, the dynamics of the converter will be independent of the output load. The benefit of the approach is its simplicity, which can be seen immediately from the model, where the gains of the robust controller play an important role. This regulator provides a non-pulsating input current; thus, it is suitable as an interface between lithium-ion batteries and on-board applications. The paper is organized as follows. The relationships that allow fair values of the converter's electric elements and stress voltage on switching devices are shown in Section 2. A detailed analysis of the converter dynamics is given in Section 3, where the equivalent series resistor (ESR) of the capacitor filter is added. The bilinear piecewise and linearized models are also derived, as well as an analysis of the effect of the input filter on the dynamics of the switching DC-DC converter and the control performance. The procedure for controller design is given in Sections 4 and 5 shows test results in the time and frequency domains for a laboratory prototype with an output power capacity of 300 W. Finally, some conclusions are discussed in Section 6.

2. Steady-State Analysis and Design of the QCIF

The QCIF is shown in Figure 3. The components of the input filter are L_{in} and C_{in}. The resulting circuits are shown in Figure 4 when switches M_1 and M_2 are open or closed. The expressions of capacitor voltages and inductor currents for the steady-state conditions are obtained under the assumption that the QCIF works in continuous conduction mode (CCM) where the parasitic of the components have been neglected for simplicity:

$$V_{C_{in}} = V_{in}, \tag{1}$$

$$V_{C_T} = V_{in}D(1 - D), \tag{2}$$

$$V_O = V_{in}D^2, \tag{3}$$

$$I_{L_{in}} = V_{in}D^4/R, \tag{4}$$

$$I_{L_1} = V_{in}D^3/R, \tag{5}$$
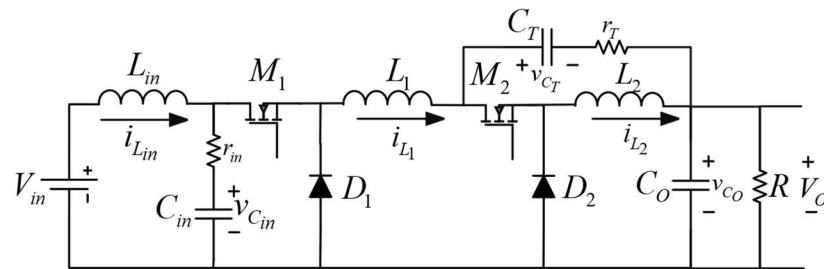
$$I_{L_2} = V_{in}D^2/R. \tag{6}$$

Figure 3. Quadratic-based step-down converter combined with an input filter (QCIF).

(**a**)

(**b**)
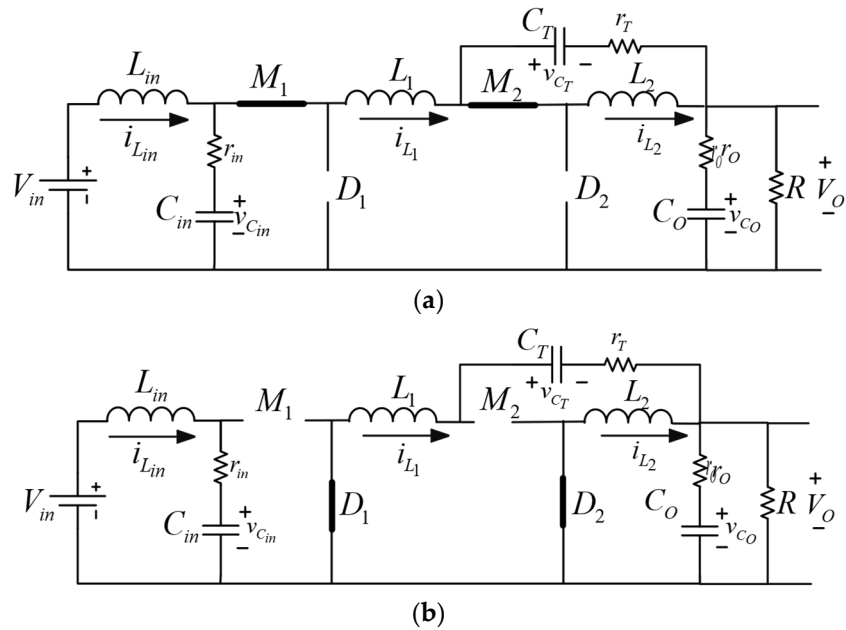
Figure 4. Electrical circuits when switches $M_{1,2}$ are: (**a**) ON or (**b**) OFF.

By assuming neglectable voltage drops on the switching devices, the current and voltage of inductors and capacitors, represented by ΔI_n and ΔV_n are:

$$\Delta I_{L_{in}} = (V_{in} - v_{C_{in}})/L_{in}f_S, \tag{7}$$

$$\Delta I_{L_1} = [V_{in}(1 - D)D]/L_1f_S, \tag{8}$$

$$\Delta I_{L_2} = [V_{in}(1 - D)D^2]/L_2f_S, \tag{9}$$

$$\Delta V_{C_T} = [V_{in}(1 - D)D^3]/C_TRf_S, \tag{10}$$

$$\Delta V_{C_O} = [V_{in}(1-D)D^3]/C_O R f_S, \tag{11}$$

where f_S is the switching frequency. For simplicity, the parasitic of the converter components are neglected in these expressions. The waveforms for the corresponding ripples are depicted in Figure 5. As can be seen, the input current provides a suitable behavior for lithium-ion batteries.
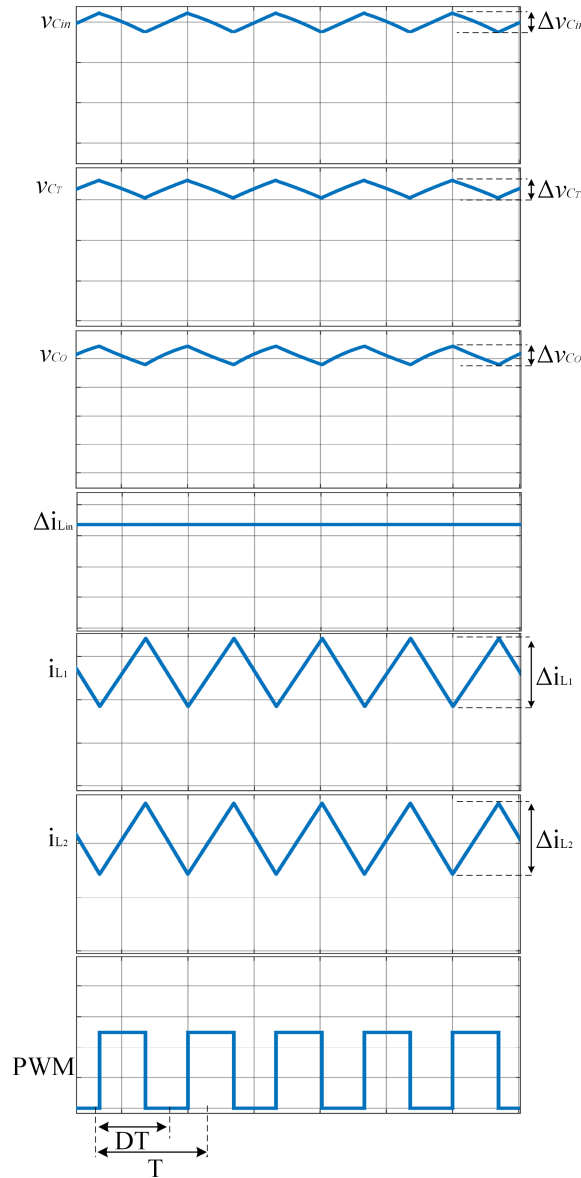
Figure 5. Waveforms of QCIF variables.

The current and voltage stresses on the MOSFETs and diodes I_{SSM_1}, I_{SSM_2}, I_{SSD_1}, I_{SSD_2}, V_{SSM_1}, V_{SSM_2}, V_{SSD_1}, and V_{SSD_2} can be computed by:

$$I_{SSM_1} = I_{SSD_1} = \left(D^2/R + (1-D)/(2L_1 f_S) \right) D V_{in}, \tag{12}$$

$$I_{SSM_2} = I_{SSD_2} = (1/R + (1-D)/(2L_2 f_S)) D^2 V_{in} \tag{13}$$

$$V_{SSM_1} = -V_{SSD_1} = V_{in}, \tag{14}$$

$$V_{SSM_2} = -V_{SSD_2} = D V_{in} \tag{15}$$

Also, the following inequality for f_{LC} and converter parameters has been proposed to avoid oscillations during transient response and improve the behavior of the QCIF [26]:

$$f_{LC} < 1/(2\pi\sqrt{L_1 C_T}) < 1/(2\pi\sqrt{L_2 C_O}) \tag{16}$$

3. Dynamic Analysis and Modelling of the QCIF

A model is obtained for each case to carry out a comparative study of the behavior of QCIF without and with the effect of ESR of the capacitors and inductors. To start with, a binary commutation function "q" is defined to represent the dynamic of QCIF by a bilinear piecewise model. The commutation function takes the values 1 and 0 when M_1 and M_2 are ON and OFF, respectively. As a result, the set of equations corresponding to the inductor currents and capacitor voltages are shown in Equation (17) without the effect of ESR and Equation (18) with the effect of ESR:

$$\left.\begin{array}{ll} \dot{i}_{L_{in}} = (V_{in} - v_{C_{in}})/L_{in}, & \dot{i}_{L_1} = -(v_{C_T} + v_{C_O} - q\,v_{C_{in}})/L_1, \\ \dot{i}_{L_2} = (q\,v_{C_T} + v_{C_O}(q-1))/L_2, & \dot{v}_{C_{in}} = (i_{L_{in}} - q\,i_{L_1})/C_{in}, \\ \dot{v}_{C_T} = (i_{L_1} - q\,i_{L_2})/C_T, & \dot{v}_{C_O} = (i_{L_1} + i_{L_2}(1-q))/C_O - v_{C_O}/(C_O R). \end{array}\right\} \tag{17}$$

$$\left.\begin{array}{l} \dot{i}_{L_{in}} = (V_{in} - i_{L_{in}}(r_{in_C} + r_{in_L}) - v_{C_{in}} + i_{L_1} r_{in_C} q)/L_{in}, \\ \dot{i}_{L_1} = -[(((v_{C_O}/R) - i_{L_1} - i_{L_2})r_O(1-q) - v_{C_T} - v_{C_O}) - i_{L_1}(r_T + r_1) + (v_{C_{in}} + i_{L_2} r_T + r_{in_C}(i_{L_{in}} - i_{L_1})q)]/L_1, \\ \dot{i}_{L_2} = (((v_{C_T} + r_T(i_{L_1} - i_{L_2}))q - i_{L_2} r_2) - ((v_{C_O}/R + i_{L_1} + i_{L_2})r_O + v_{C_O})(1-q))/L_1 \\ \dot{v}_{C_{in}} = (i_{L_{in}} - q i_{L_1})/C_{in}, \qquad \dot{v}_{C_T} = (i_{L_1} - q i_{L_2})/C_T, \\ \dot{v}_{C_O} = (i_{L_1} + i_{L_2}(1-q))/C_O - v_{C_O}/(C_O R). \end{array}\right\} \tag{18}$$

It is well-known that high-frequency switching DC/DC converters can be approximated by their corresponding low-frequency continuous model. By averaging the q function and the state-space equations of the bilinear piecewise model, the related time-average functions with the form:

$$\dot{x} = \overline{A}(d)x + \overline{B}(d)v_{in} \tag{19}$$

are obtained. In this expression, $x \,\epsilon\, R^6$ is the state vector, $v_{in} \in R$ is the input voltage, $\bar{A} \,\epsilon\, R^{6\times6}$ is a matrix, $\overline{B} \,\epsilon\, R^6$ is the input vector, and $d(t)$ is the duty cycle. As can be seen, the matrix and the input vector are influenced by the duty cycle d, so the set of equations is nonlinear.

By applying linearization techniques to nonlinear models, it is possible to describe the behavior of the converter. These models are linearized around the operating point corresponding to the steady-state values given by (1) to (6). The procedure to derive it is as follows. The input voltage, control signal, and six state variables are divided into two parts: the nominal average values, which are denoted by upper-case letters, and variations of their nominal operating point, which are denoted by lower case with a superscript "$\sim$".

$$x = X + \widetilde{x}, \; d = D + \widetilde{d}, \; v_{in} = V_{in} + \widetilde{v}_{in} \tag{20}$$

Then, the Equation (19) are rewrite in terms of the disturbed variables of Equation (20). The products of disturbance are not considered, since these are of second order. Finally in these equations, the values of the constant parameters are substituted by the nominal values of variables. The linear models without Equation (21) and with Equation (22) of the ESR of capacitors and inductors are obtained:

$$\begin{bmatrix} \dot{\widetilde{i}}_{L_{in}} \\ \dot{\widetilde{i}}_{L_1} \\ \dot{\widetilde{i}}_{L_2} \\ \dot{\widetilde{v}}_{C_{in}} \\ \dot{\widetilde{v}}_{C_T} \\ \dot{\widetilde{v}}_{C_O} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1/L_{in} & 0 & 0 \\ 0 & 0 & 0 & D/L_1 & -1/L_1 & -1/L_1 \\ 0 & 0 & 0 & 0 & D/L_2 & (D-1)/L_2 \\ 1/C_{in} & -D/C_{in} & 0 & 0 & 0 & 0 \\ 0 & 1/C_T & -D/C_T & 0 & 0 & 0 \\ 0 & 1/C_O & (1-D)/C_O & 0 & 0 & -1/RC_O \end{bmatrix} \begin{bmatrix} \widetilde{i}_{L_{in}} \\ \widetilde{i}_{L_1} \\ \widetilde{i}_{L_2} \\ \widetilde{v}_{C_{in}} \\ \widetilde{v}_{C_T} \\ \widetilde{v}_{C_O} \end{bmatrix} + \begin{bmatrix} 0 \\ V_{in}/L_1 \\ DV_{in}/L_2 \\ -D^3 V_{in}/C_{in} R \\ -D^2 V_{in}/C_T R \\ -D^2 V_{in}/C_O R \end{bmatrix} \widetilde{u} \tag{21}$$

$$
\begin{bmatrix}
\dot{\tilde{i}}_{L_{in}} \\
\dot{\tilde{i}}_{L_1} \\
\dot{\tilde{i}}_{L_2} \\
\dot{\tilde{v}}_{C_{in}} \\
\dot{\tilde{v}}_{C_T} \\
\dot{\tilde{v}}_{C_O}
\end{bmatrix}
=
\begin{bmatrix}
-(r_{in_C}+r_{in_L})/L_{in} & Dr_{in}/L_{in} & 0 & -1/L_{in} & 0 & 0 \\
(Dr_{in_C})/L_1 & -(r_T+r_1+Dr_{in_C}+r_O(1-D))/L_1 & (Dr_T-r_O(1-D))/L_1 & D/L_1 & -1/L_1 & (R+r_O(1-D))/RL_1 \\
0 & (Dr_T-r_O(1-D))/L_2 & -(r_2+Dr_T+r_O(1-D))/L_2 & 0 & D/L_2 & (R+(1-D)r_O)/RL_2 \\
1/C_{in} & -D/C_{in} & 0 & 0 & 0 & 0 \\
0 & 1/C_T & -D/C_T & 0 & 0 & 0 \\
0 & 1/C_O & (1-D)/C_O & 0 & 0 & -1/(RC_O)
\end{bmatrix}
\begin{bmatrix}
\tilde{i}_{L_{in}} \\
\tilde{i}_{L_1} \\
\tilde{i}_{L_2} \\
\tilde{v}_{C_{in}} \\
\tilde{v}_{C_T} \\
\tilde{v}_{C_O}
\end{bmatrix}
$$

$$
+
\begin{bmatrix}
(I_{L_1}r_{in_C})/L_{in} \\
(V_{C_{in}}+I_{L_2}r_T-r_{in_C}(I_{L_1}-I_{L_{in}})+r_O(I_{L_1}+I_{L_2}-V_{C_O}/R))/L_1 \\
(V_{C_T}+V_{C_O}+r_T(I_{L_1}-I_{L_2})+r_O(I_{L_1}+I_{L_2}+V_{C_O}/R))/L_2 \\
-I_{L_1}/C_{in} \\
-I_{L_2}/C_T \\
-I_{L_2}/C_O
\end{bmatrix}
\tilde{u}
\tag{22}
$$

Based on the resulting linear models, the Laplace transforms are applied to analyze the dynamic behavior of the QCIF. This analysis mainly focuses on the transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ to determine the effect that the electric elements and ESR of the input filter capacitor have on the dynamic behavior of the QCIF and its output voltage. The resulting transfer function has the form:

$$
\frac{\tilde{v}_O(s)}{\tilde{d}(s)} = \frac{-b_5s^5 + b_4s^4 - b_3\,s^3 + b_2s^2 - b_1s + b_0}{s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}
\tag{23}
$$

where a_i and b_i with $i = 0\ldots5$ are the denominator and numerator polynomial coefficients. The expressions for the coefficients are too large, so they are omitted here due to space limitations; however, numerical results are shown in Section 5.

The converter is stable and has non-minimum phase behavior; however, if the ESR of the capacitor input filter is added to the model, the coefficients b_5, b_3, and b_1 become positive, which reduces the number of zeros on the right-hand side (RHS) of the s-plane. Furthermore, in physical applications, this characteristic can exhibit different values depending on the dielectric used in the capacitor by the manufacturer.

Despite this change, the transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ has non-minimum phase behavior because it continues to have zeros on the right-hand side (RHS) of the s-plane. For this reason, it is very difficult to achieve good closed-loop performance with only the voltage loop due to resonant peaks and abrupt phase changes [28]. The transfer function $\tilde{i}_{L_1}(s)/\tilde{d}(s)$ was also obtained:

$$
\frac{\tilde{i}_{L_1}(s)}{\tilde{d}(s)} = \frac{c_4s^4 + c_3\,s^3 + c_2s^2 + c_1s + c_0}{s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}
\tag{24}
$$

It has the same poles as $\tilde{v}_O(s)/\tilde{d}(s)$ but all its zeros are located in the LHS of the plane, thus it has minimal phase behavior. For this reason, i_{L1} is a variable to consider when implementing a control system. In Section 5, the numerical results are shown.

Finally, it is necessary to design the input filter to carry out an adequate design of the converter. The criterion is that it has to satisfy the following inequality [26]:

$$
Z_f(s) < Z_C(s)
\tag{25}
$$

where $Z_f(s)$ is the output impedance of the input filter, and $Z_C(s)$ is the input impedance of the converter. Their corresponding values are computed by:

$$
Z_f(s) = \frac{(C_{in}L_{in}r_{in})s^2 + L_{in}s}{(C_{in}L_{in})s^2 + (C_{in}r_{in})s + 1},
\tag{26}
$$

$$
Z_C^{-1}(s) = \frac{e_4s^4 + e_3s^3 + e_2s^2 + e_1s + R}{s^3 + g_2s^2 + g_1s + D^4},
\tag{27}
$$

where $e_4 = (C_TC_OL_1L_2R), e_3 = (C_TL_1L_2),$

$$
e_2 = \big(((1 + D^2 - 2D)L_1 + L_2)C_TR + (L_2 + L_1D^2)C_OR\big),
$$

$$e_1 = \left(L_1 D^2 + L_2\right), g_3 = \left(C_T C_O L_2 R D^2\right), g_2 = \left(C_T L_2 D^2\right)$$

$$g_1 = \left(\left(1 - 2D + D^3\right) C_T R D^2 + C_O R D^4\right)$$

The expression of the input impedance of the converter is obtained from the transfer function input voltage to input current $v_{in}(s)/i_{in}(s)$ [26] obtained from the state-space average linear model of QBC without filter, shown in Figure 2, in which the input current of the converter is given by $\tilde{i}_{L_1}$.

Therefore, attention should be taken to satisfy the inequalities given in Equation (25). Once the impedance of the input filter has been ensured, the controller for the QCIF can be designed.

4. Controller Design for the Converter QCIF

The controller must efficiently mitigate the voltage changes in the output produced by the operational conditions, for example, changes in input source voltage and output load. When lithium-ion batteries are used, they exhibit voltage variations up to 15% of their nominal value. These variations depend on some factors: charging state, operating temperature, and nominal voltage, among others [7,29,30]. Therefore, the controller should also compensate for the parametric uncertainties and nonlinearities presented by the QCIF. The two primary control approaches are voltage-mode control and current-mode control. The latter exhibits advantages over the voltage-mode control because sensing the current of the input inductor improves the transient response and protects against current overloads of the input power.

As mentioned in the above section, the stability is quite difficult to achieve when the transfer function $\tilde{v}_O(s)/\tilde{d}(s)$ has RHS zeros. Moreover, selecting the inductor current that will be used for the internal loop is crucial from performance and implementation viewpoints. It was shown the transfer function first-stage inductor-to-duty cycle of the converter has minimum phase behavior, so it is appropriate for the internal current loop. Furthermore, this selection is appropriate to design the control loop with the highest gain and bandwidth; thus, the advantages of current-mode control are ensured. The block diagram for the control scheme is shown in Figure 6, where V_{ramp} is a ramp waveform, which is compared with the control signal. A low-pass filter F(s) has a high-frequency pole, a high-gain compensator G(s) is added in the internal current loop, V_{ref} is the desired voltage, N and H are the current and voltage sensor gains, and PI is the controller of the external voltage loop.
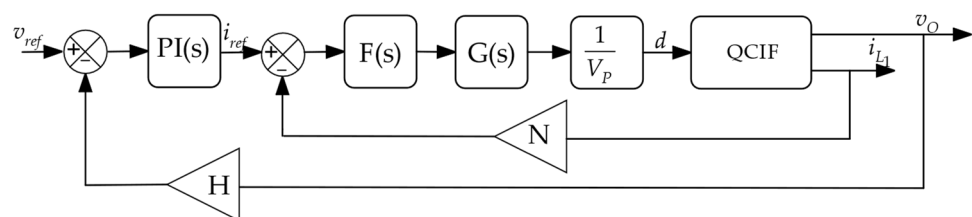

Figure 6. Control scheme block diagram.

The control system design criteria are based on the loop-shaping technique. The following conditions should be satisfied for good performance of the switching regulator:

1. To reduce the sensitivity, the slope at the crossover frequency of the voltage loop gain must be approximately -20 dB/dec
2. For voltage regulation, the voltage loop gain should be high at low frequencies and low at high frequencies
3. For better speed response, the bandwidth should be large.
4. For robustness, good gain and phase margins are required.

The above conditions should be satisfied with the two control loops of the current-mode control; however, the PI-controller of the outer voltage loop plays an important role. The pole of PI-controller helps for voltage regulation and robustness. The zero of the PI-controller helps to reduce sensitivity and better speed response. The gain and phase margins should be positive if a closed-loop system is stable. In general, gain margins of 2–10 dB and phase margins of 30–60 degrees are desirable tradeoffs between bandwidth and stability in the closed-loop system design.

The procedure to design each loop, select the appropriate value of gains, and therefore choose the components of the controller circuit, are described below:

4.1. Internal Current Loop Design

At first, the internal loop, or current loop, is designed. It produces a faster transient response and, as noted in Figure 6, consists of low-pass filter F(s) and a high-gain compensator G(s), with the following transfer functions:

$$G(s) = G_P(s + \omega_Z)/s, \quad F(s) = 1/(s/\omega_P + 1), \tag{28}$$

respectively, where ω_Z is the location of the compensator zero whose value is given by $\omega_Z = 1/R_F C_{FZ}$. It must be placed at a frequency lower than that at which the LC filters produced naturally by the inductors and capacitors of the converter are located. Therefore, in practice is placed at least a decade below half the switching frequency of the converter, thus, the value of the resistor R_F and capacitor C_F can be calculated. The gain G_P of the compensator is given by $G_P = R_F/R_1$, and it has to satisfy the following inequality:

$$G_P < (5RV_{ramp})/(3D^2 V_{in} N), \tag{29}$$

Thus, from this expression, it is possible to calculate the value of R_1.

To provide noise immunity from the inductor current, the high-frequency pole of $F(s)$ is placed at a frequency equal to or above half the switching frequency and can be computed by $\omega_P = (C_{FZ} + C_{FP})/R_F C_{FZ} C_{FP}$. From this expression, the capacitor C_{FZ} can be calculated.

Thus, the control law is given by:

$$\widetilde{u} = \left(\frac{G_P(s + \omega_Z)}{s} \right) \left(\frac{1}{s/\omega_P + 1} \right) \left(\frac{1}{V_{ramp}} \right) \left(\widetilde{i}_{ref} - N\widetilde{i}_{L_1} \right), \tag{30}$$

4.2. External Voltage Loop Design

Once the internal loop has been tuned, the external or voltage loop of the controller, is designed. It is composed of a voltage sensor with a gain H and a PI controller with a transfer function given by:

$$PI(s) = K_C(1 + (1/T_i s)), \tag{31}$$

where T_i and K_C are the integral time in seconds given by $T_i = R_{FC} C_{FC}$ and proportional gain given by $K_C = R_{FC}/R_2$ respectively. The purpose of $PI(s)$ is to provide a high gain to the controller at low frequencies; thus, the value of resistor R_{FC} and capacitor C_{FC} must be selected such that $1/T_i$ is placed at least one decade below the converter switching frequency. The gain is set to obtain the appropriate gain and phase margins of the voltage loop by the expression

$$K_P < \frac{2ND}{HR(1 - D)} \tag{32}$$

This gain is adjusted in the controller circuit by RFC/R1C. It is important to notice that expressions (30) and (33) provide a first approximation of internal and external loop controller gains; subsequently, an iterative tuning process has to be carried out to guarantee the appropriate robust stability of the regulator.

The expression of this loop, in the physical regulator is given by:

$$\tilde{i}_{ref} = K_C \left(1 + \frac{1}{T_i s}\right)\left(\tilde{v}_{ref} - H\tilde{v}_O\right), \tag{33}$$

The electrical circuit of the proposed scheme controller for the QCIF can be implemented as depicted in Figure 7. A flow chart showing the steps that must be performed to design, calculate, implement and experimentally verify the performance of the switching regulator based on the pro-posed converter model is depicted in Figure 8.
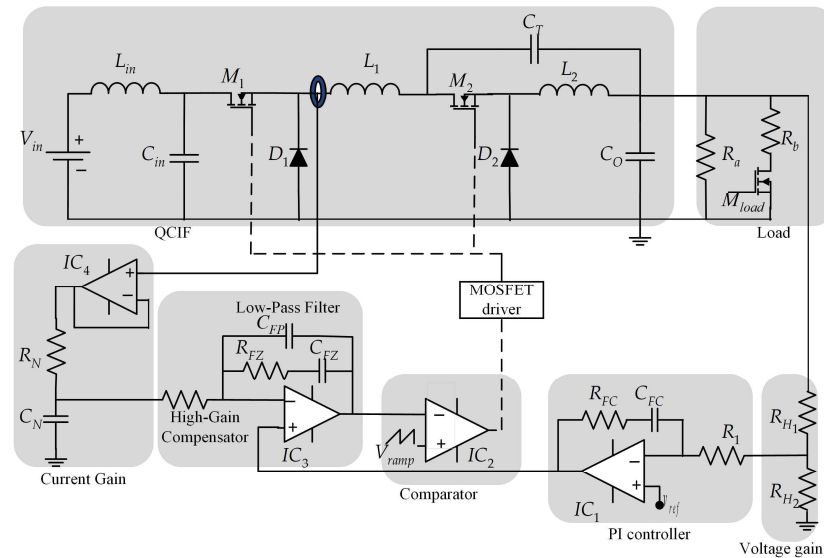

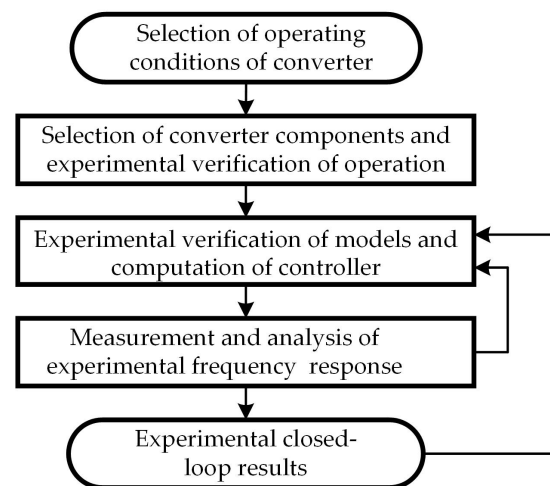**Figure 7.** Diagram of the controller of the QCIF.

Figure 8. Switching regulator design process flowchart.

5. Experimental Results

A QCIF was built in the laboratory to validate the theoretical development with the nominal conditions for the on-board converter of a hybrid electric vehicle: an input voltage of 48V, an output voltage of 12 V, and an output power of 300 W. The parameters of the converter are given in Table 1, in which the duty cycle to be used is defined from the relationship between the output and the input voltage given by $V_O = V_{in}D^2$. Because the switching frequency is a factor to consider in the design of the inductors to be used according to the relationships given by Equations (7)–(9), there should be an adequate relationship between the size of the inductor and the current that flows through it, determined by the

power handled. The switching frequency of the converter should be greater than 20 kHz to prevent noise from being captured by the human ear.

Table 1. Parameters of the converter.

Parameter	Quantity
Input voltage	48 V
Output voltage	12 V
Duty cycle	0.5
ΔV_{CO}	0.5%
ΔI_{L1} and ΔI_{L2}	25%
Switching frequency	75 kHz

The corresponding values of the elements are given in Table 2. MOSFET elements with low on-state resistance, high current handling capacity, and reduced drain-source voltage are selected as active switches. In the case of passive switches, Schottky-type di-odes were used due to their low forward voltage drop, minimal switching losses, low voltage peak magnitudes, as well as ultra-fast recovery. The current and voltage characteristics of the devices are given in Table 2. A photo of the prototype is depicted in Figure 9.

Table 2. Elements of converter.

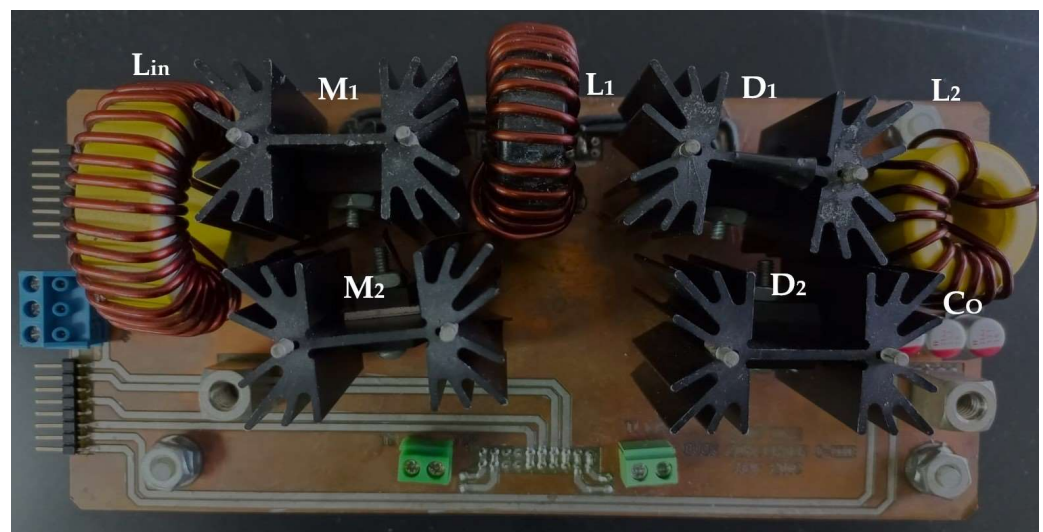| Component	Value/Model	Component	Value/Model
C_{in}	940 μF	r_{inL}	0.020 Ω
C_T	990 μF	r_{L1}	0.060 Ω
C_O	1320 μF	r_{L2}	0.040 Ω
$r_{C_{in}}$	0.054 Ω	R	0.48 Ω
r_{C_T}	0.0037 Ω	M_1	IRFP4468, 100 V, 290 A
r_{C_O}	0.0029 Ω	M_2	IRFP4004 40 V, 350 A
L_{in}	65 μH	D_1	DSA120C150QB 150 V, 120 A
L_1	52 μH	D_2	DSSK80-006B 60 V, 40 A
L_2	13 μH	IC1to IC4	TL81
		Comparator	LM311

Figure 9. Photo of laboratory prototype.

The transfer functions $\widetilde{i}_{L_1}(s)/\widetilde{d}(s)$ and $\widetilde{v}_O(s)/\widetilde{d}(s)$ were calculated numerically by substituting the values of the components of the QCFI from Table 2 into the linear models of the converter without and with ESR given by expressions (22) and (23). These transfer functions were obtained using the ss2tf command of the Matlab® software for ease. Subsequently, the zeros and poles of each transfer function were obtained, which are shown in Table 3. As can be seen, the effect of ESR reduces the number of zeros of the transfer function $\widetilde{v}_O(s)/\widetilde{d}(s)$ on the right-hand side (RHS) of the s-plane, and produces only zeros on the left-hand side of transfer function $\widetilde{i}_{L_1}(s)/\widetilde{d}(s)$, making the first-inductor current, suitable to be fed back into the current loop.

Table 3. Poles and zeros of transfer functions of QCFI.

ESR Value	Poles	Zeros $\widetilde{v}_O(s)/\widetilde{d}(s)$	Zeros $\widetilde{i}_{L_1}(s)/\widetilde{d}(s)$
without	$\begin{cases} -6 \pm 7676.5i \\ -629 \pm 5704i \\ -166 \pm 3698i \end{cases}$	$\begin{cases} 73,742 \\ -18 \pm 7647i \\ 70 \pm 3924i \end{cases}$	$\begin{cases} -2344 \\ 42 \pm 4064i \\ -61 \pm 6262i \end{cases}$
0.054 Ω	$\begin{cases} -353 \pm 6223i \\ -705 \pm 5728i \\ -405 \pm 3600i \end{cases}$	$\begin{cases} 73,488 \\ -236 \pm 6522i \\ -259 \pm 3863i \end{cases}$	$\begin{cases} -2314 \\ -61 \pm 6269i \\ -380 \pm 4054i \end{cases}$

5.1. Open Loop Test Results

The proposed theoretical models of QCFI were validated in the laboratory using the frequency response Analyzer 300 AP. The theoretical frequency response of the transfer function of the first inductor current-to-duty cycle is compared with the corresponding experimental and shown in Figure 10.
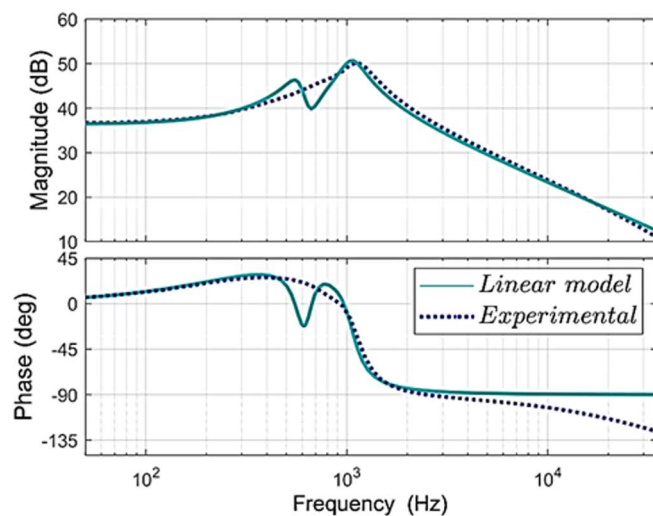

Figure 10. Frequency response of $\widetilde{i}_{L_1}(s)/\widetilde{d}(s)$ for the linear model and experimental open loop circuit.

A high damping can be observed in the experimental response due to the parasitic resistances, as mentioned in Section 3. The phase plot corresponds to a minimum phase transfer function suitable for designing a controller. The similarity between the two responses is remarkable. The theoretical and experimental frequency responses of the output voltage–to–duty cycle are shown in Figure 11. The significant change in phase shows the existence of right-hand zeros in the transfer function. Both plots are very close. The proposed model accurately predicts the actual behavior of the QCIF and allows the model to be validated through the experimental frequency response. These models can be used to design a robust controller.
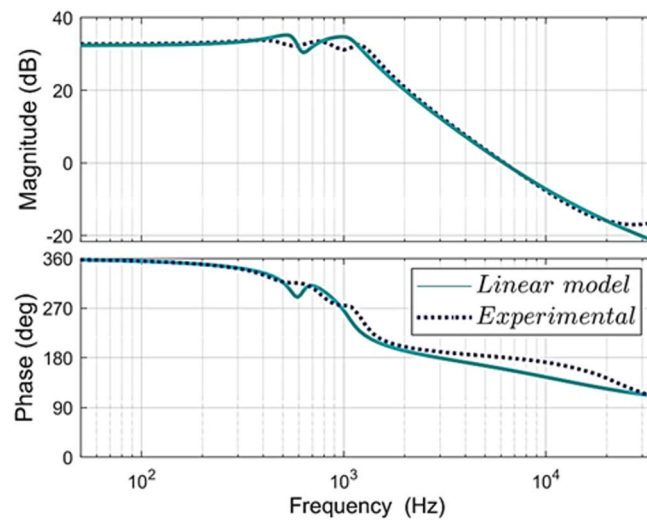
Figure 11. Frequency response of $\tilde{v}_O(s)/\tilde{d}(s)$ for the linear model and experimental open loop circuit.

The first tests were taken in an open loop by adjusting the duty ratio to 0.5 to obtain the nominal operation. The inductor current and capacitor voltage of the input filter are shown in Figure 12; as can be seen, the input current to the converter has a value of approximately 6.5 A and does not have a pulsating waveform. This is suitable for processing energy from lithium-ion batteries. The current flowing through inductors L_1 and L_2 are depicted in Figure 13; these signals were obtained using the Tektronix TCPA AC/DC series current measurement probes. The experimental waveforms have a sawtooth form, as predicted. The capacitor voltages $v_{C_{in}}$, v_{C_T}, and v_{C_O} are depicted in Figure 14. The voltages in the transfer capacitor and the output voltage have a value of 12 V voltage, as predicted. To appreciate the ripple in the output voltage, a zoom is obtained and shown in Figure 15. The resulting ripple is about 90 mV, where the ESR effect of the output capacitor can be noticed. Finally, a summary of the ripples obtained analytically and experimentally is shown in Table 4.
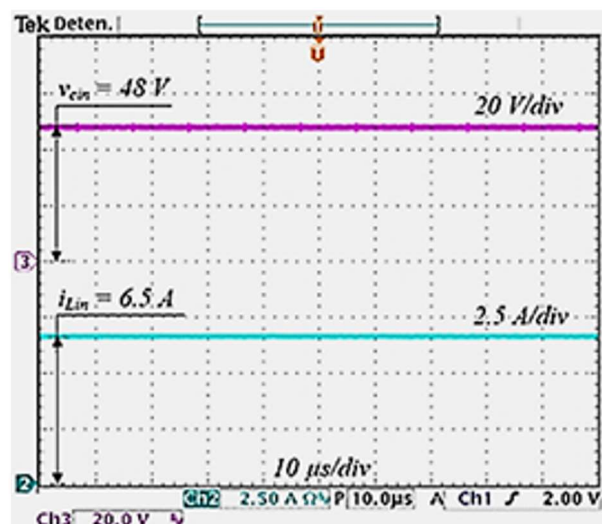

Figure 12. Experimental waveforms of the input filter: (**top**) capacitor voltage $v_{C_{in}}$ (y-axis: 20 V/div), and (**bottom**) inductor current $i_{L_{in}}$ (y-axis: 2.5 A/div), (x-axis: time 10 μs/div).
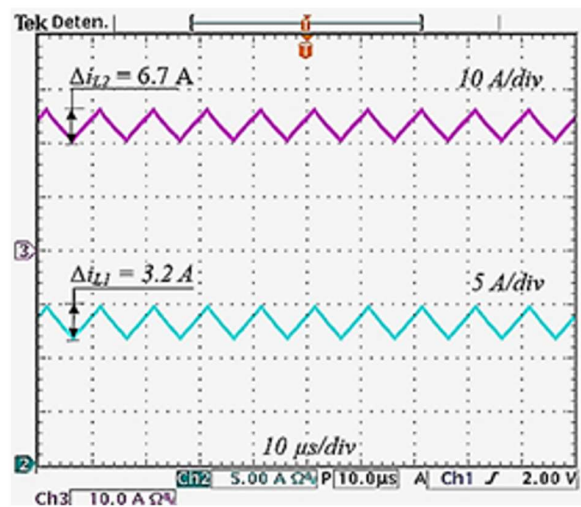
Figure 13. Experimental inductor current waveforms of the prototype: (**top**) inductor current i_{L_2} (*y*-axis: 10 A/div), and (**bottom**) inductor current i_{L_1} (*y*-axis: 5 A/div), (*x*-axis: time 10 μs/div).
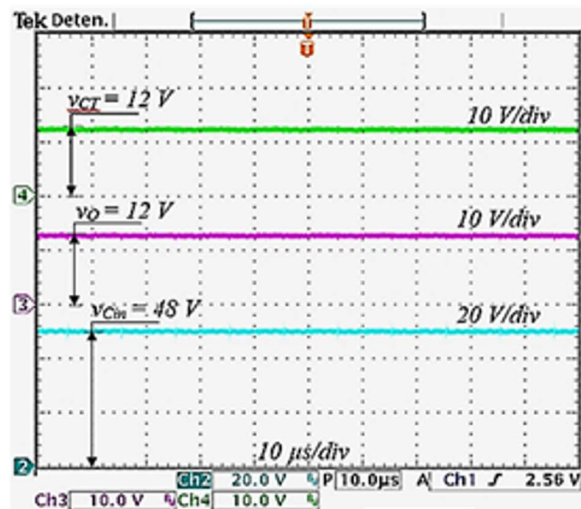

Figure 14. Experimental capacitor voltages: (From (**top**) to (**bottom**)) v_{C_T} (*y*-axis 10 V/div), v_O (*y*-axis 10 V/div) and $v_{C_{in}}$ (*y*-axis 20 V/div), (*x*-axis: time 10 μs/div).
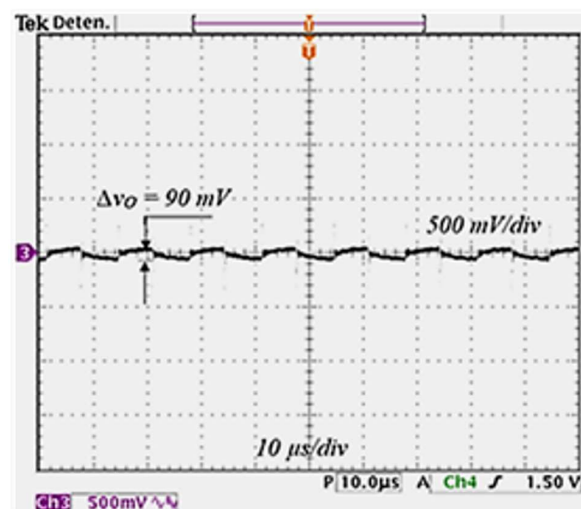

Figure 15. Experimental voltage ripple of output voltage: v_O (*y*-axis 500 mV/div), (*x*-axis: time 10 μs/div).

Table 4. Ripple comparison.

Ripple	Analytical			Experimental		
	DC Value	Value	% DC Value	DC Value	Value	% DC Value
ΔI_{L1}	12.5 A	3.1 A	25%	13 A	3.2 A	24%
ΔI_{L2}	25 A	6.2 A	25%	24 A	6.7 A	28%
ΔI_{Co}	12 V	60 mV	0.5%	12 V	90 mV	0.7%

The behavior of the QCIF was examined in open loop to determine how step changes in load are reflected in the output voltage. The above was done by connecting an extra load in parallel to the nominal load, as shown in Figure 7. Then, a square signal was applied to MOSFET M at a frequency of 5 Hz. The load demands a current of 25 A when the MOSFET is ON and 5 A when it is OFF. The above represents a power consumption of 300 W (100% of rated output power) and 60 W (20% of rated output power). The output voltage response to these load variations is shown in Figure 16. As can be seen, the output voltage reaches 14 V.
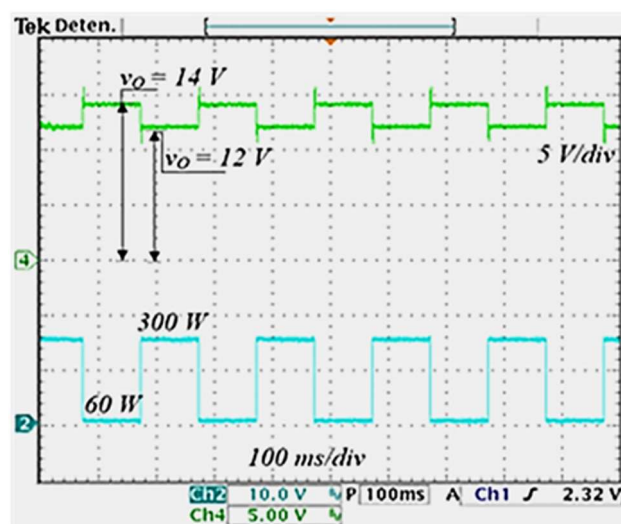

Figure 16. Experimental open-loop response to step changes in the load: (**top**) Output voltage of converter v_O (*y*-axis: 5 V/div), and (**bottom**) V gate voltage of the MOSFET M_{load} that changes the load from 60 W to 300 W (*y*-axis: 10 V/div) (*x*-axis: time 100 ms/div).

The efficiency of the converter at the rated output power of 300 W is defined as $\eta = P_O/P_{in}$. This value was obtained using the voltage and current data shown in Figures 12–14. The resulting efficiency of the QCIF is about 91%. However, when SiC or GaN power MOSFETs are used, the efficiency can be improved since they have lower on-resistances and better performance [31]. Efficiencies of quadratic converters with different nominal powers reported in the open literature are shown in Table 5.

Table 5. Efficiency comparison.

Converter	Input Voltage	Output Voltage	Output Power	Eff. %
Proposed QCIF	48 *V*	12 *V*	300 *W*	91
Switched-capacitor QBC [16]	36 *V*	1.5 *V*	30 *W*	75
Single-switch QBC [23]	97 *V*	5 *V*	25 *W*	80
Two-switch QBC [23]	97 *V*	5 *V*	25 *W*	78
Single-switch Semi-QBC [32]	60 *V*	36 *V*	100 *W*	84
QBC (LED applications) [33]	191 *V*	170 *V*	7 *W*	82
QBC in CCM [34] (simulated results)	24 *V*	10 *V*	10 *W*	90

5.2. Closed-Loop Test Results

The control scheme applied to the QCIF was designed according to the criteria mentioned in Section 4. The regulator values are shown in Table 6. The gain *H* for the voltage sensor was implemented in the laboratory with a voltage divider. A Hall Effect current transducer was used to sense the first inductor current, specifically the LA-55P model from the LEM company.

Table 6. Regulator values.

Component	Value	Parameter	Value
R_F	$10\,k\Omega$	ω_Z	$1.5\,kHz$
R_1	$15\,k\Omega$	G_P	0.6
C_{FP}	$150\,pF$	ω_P	$54\,kHz$
C_{FZ}	$10\,\eta F$	N	0.1
C_{FC}	$33\,nF$	K_C	0.8
R_{FC}	$2.2\,k\Omega$	ω_C	$2.1\,kH$
R_2	$2.7\,k\Omega$	H	1
R_{H1}	$18\,k\Omega$		
R_{H2}	$30\,k\Omega$		

The performance when the controller is enabled was analyzed in time and frequency domains. A comparison between the experimental closed-loop frequency response and the closed-loop linear model Bode plot is shown in Figure 17.
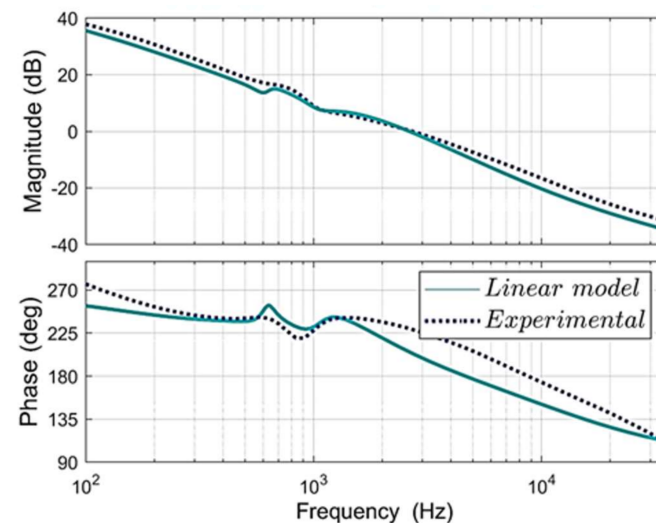

Figure 17. The frequency response for the voltage loop gain with controller enabled for the linear model and the prototype.

For both cases, the PI controller dominates the loop gain at low frequencies and has a slope of approximately 20 dB/dec at the crossover frequency. When the linear model is used, the loop gain has a 2.5 kHz bandwidth and phase and gain margins of 28 degrees and 9.5 dB, respectively. Furthermore, the response of the laboratory prototype has a bandwidth of 3.7 kHz; therefore, the regulator has a good response speed. The phase and gain margins are 38 degrees and 12 dB, respectively; thus, robust stability of the regulator is ensured.

With the controller enabled, the same step load changes used in the open loop were now applied to QCIF for the time domain test. The experimental response is depicted in Figure 18. Additionally, experimental tests were performed for variations in the input voltage from 40 V to 53 V, corresponding to the voltage variations that a nominal 48 V lithium-ion battery can reach. These variations were injected sinusoidally at 2 Hz. The behavior of the output voltage for these variations is shown in Figure 19. As can be seen, no voltage variation appears when load and input voltage changes are applied because the

good characteristics were achieved in the control loop design. The resulting bandwidth improves the response speed to changes in the load. In addition, the slope at the crossover frequency of the voltage loop gain indicates good behavior of the sensibility function, and the gain and phase margins improve robustness.
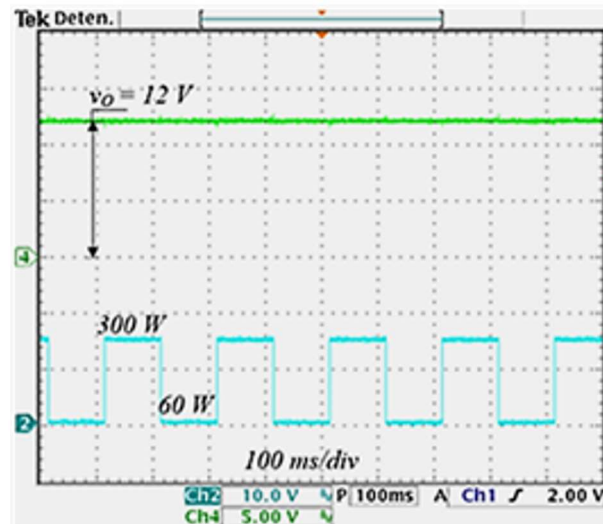

Figure 18. Experimental closed-loop response to step changes in the load: (**top**) Output voltage of converter (*y*-axis: 5 V/div), and (**bottom**) $V_{M_{load}}$ gate voltage of the MOSFET M_{load} that changes the load from 60 W to 300 W (*y*-axis: 10 V/div) (*x*-axis: time 100 ms/div).
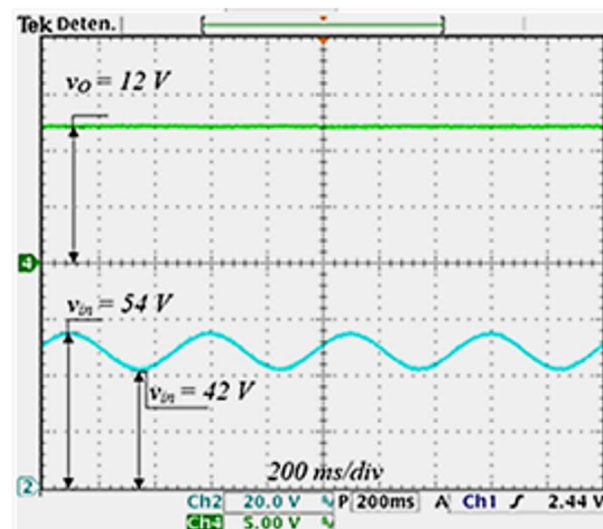

Figure 19. Experimental closed-loop response of the output voltage to input voltage variation: (**top**) output voltage (*y*-axis: 5 V/div), and (**bottom**) input voltage variation v_{in} (*y*-axis: 20 V/div), (*x*-axis: time 200 ms/div).

With the idea that the proposed switching regulator could be integrated as a module to be connected to the on-board equipment, the present work implemented the controller using an analog circuit consisting of two operational amplifiers, resistors, and capacitors. The controller is very compact and simple. However, the proposed controller could be implemented digitally using a programmable microcontroller. In this case, it is possible to incorporate other techniques to design the controller used to implement the current-mode control scheme. For example, controller optimization and efficiency methods, such as the one proposed in [35], stand out. It combines a fractional-order proportional-integral-derivative (FOPID) controller with a metaheuristic algorithm, an improved version of the Hunger Games search, as well as the help of the Nelder-Mead Method and a random

learning mechanism, to optimize its tuning. Although this scheme is implemented in a one-stage step-down converter, which presents a minimal phase dynamic response so that it can be controlled in a voltage-mode scheme, unlike the proposed converter, it does open the interest of adapting this method to the current-mode control scheme.

6. Conclusions

Lithium-ion batteries with an output voltage of 48 V or more are preferred in hybrid electric vehicles to supply the required electric power. Thus, a DC/DC converter regulated by a control scheme is necessary to feed this voltage to on-board equipment typically powered by 12 V. The proposed converter offers a wide conversion ratio and considerably improves efficiency compared to the QBCs found in the open literature. In the specific case of on-board applications that require a nominal 12 V, it can even handle an input voltage of 700 V, using a D = 0.125 duty cycle that ensures proper operation of the switching devices. An LC input filter is incorporated into this topology to obtain a non-pulsating input current since an electrical supply with a non-pulsating current demand is required. Specifications on control systems typically include stability of the closed loop system, robustness to parameter uncertainties, and ability to follow reference signals. To design the appropriate control scheme, the transfer functions of the converter are obtained, including the effect produced by the input filter on the dynamics of the converter. In addition, the required conditions are given to design the input filter of the converter correctly. The approximate nature of mathematical models and the imperfect knowledge of the system parameters make it difficult to design a robust controller. The loop-shaping technique can be selected to design a robust controller with suitable gain and phase margins. The authors strongly believe that this approach is valuable and easy to understand and, despite its relative simplicity, gives results that are accurate enough for practical applications. Implementing the proposed controller is easy and also can be done digitally. Finally, experimental tests in the time and frequency domains validate the proposed models and show that the designed controller provides robust stability under battery voltage varia-tions and load changes.

Author Contributions: C.A.A.-F.: Methodology, formal analysis, investigation, writing—original draft preparation. J.L.-R.: Visualization, supervision, project administration. M.G.O.-L.: Validation, writing—review and editing. L.H.D.-S.: Experimental results. All authors have read and agreed to the published version of the manuscript.

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest: The authors declare no conflict of interest.

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