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Control Strategy of a Quadratic Boost Converter with Voltage Multiplier Cell for High Voltage Gain

J. Leyva-Ramos, *Senior Member, IEEE*, R. Mota-Varona, M. G. Ortiz-Lopez, *Member, IEEE*, L. H. Diaz-Saldierna, and D. Langarica-Cordoba

***Abstract*— The need of DC-DC switching converters for power supplies with high voltage gains has increased in the recent years due to new applications in areas as renewable energy systems, transportation, industrial, medical and others. A quadratic boost converter is a useful topology to obtain a step-up output voltage; however, a major drawback is the presence of a higher voltage stress over the active and passive switches. In this work, a quadratic boost converter is combined with a voltage multiplier cell and an output filter to offer a high voltage gain converter with non-pulsating input and output currents. The expressions for the capacitor voltages and inductor currents are given, as well as the corresponding ripples that allow the proper design of the converter. The bilinear switched, nonlinear averaged and linear averaged models are derived such that the dynamical behavior of the converter is analyzed and used to design a control strategy. A step-by-step procedure is given to tune up a current-mode controller. Experimental results are shown from a prototype, which delivers an output voltage of 220 V and an output power of 300 W. Step load changes between 20% and full load are applied to exhibit the robustness of switching regulator.**

***Index Terms*— Quadratic boost converter, voltage multiplier cell, switching regulator, high voltage gain.**

I. Introduction

Multiple new applications are requiring high step-up converters for equipment such as photovoltaic and fuel cell stacks, uninterruptible power supplies, X-ray systems, TV-CRT´s, high-density discharge lamps of automobile headlamps, among others [1-6]. The first option to be considered for a step-up voltage is the use of a conventional boost converter. The major drawback is the need of a relative large duty cycle for a high voltage gain, which causes a deterioration of the output voltage and control signal. To satisfy the demand of high boost applications, several topologies of DC-DC converters have been proposed in the open literature such as cascaded, multilevel, interleaved, voltage multipliers, switched-capacitor/inductor and coupled inductors [7].

The cascade converter is a simple approach to increase the voltage gain, which consists of two or more basic DC-DC converters connected in cascade with the corresponding increase in power losses and voltage stress on the switching devices [8, 9]. A cascade boost converter consisting of two boost converters operating at different frequencies has been proposed in [10]. The voltage stress on its first stage is relatively low; therefore, it can operate at high frequencies. On the other hand, its second stage can operate at low frequencies to reduce the switching losses; however, multiple active switches and different operating frequencies can make difficult the implementation of a control scheme for the converter in a switching regulator.

A very interesting kind of cascade converter is the quadratic with a single active switch, where the voltage ratio is given as a quadratic function of the duty cycle [11, 12]. Quadratic and cubic boost converters are studied in [13, 14], which have fourth and sixth-order dynamic behavior. Then, the above converters are used in switching regulators where the tuning procedure of the controllers is given by trial and error. Modified schemes of quadratic converters that produce low stress in capacitors have been also proposed [15]. A comparative study between boost, quadratic boost and cubic boost converters shows that the quadratic boost converter provides the best trade-off between duty ratio range and converter efficiency. Then, a two loop sliding-mode control is proposed to regulate the output voltage in a quadratic converter to be used for a photovoltaic panel [16].

To obtain higher voltage gains, quadratic converters can be combined with multiplier modules, see [17], where a quadratic boost converter is used in the first stage and a coupled inductor module with a series connection of output capacitors in the second stage. Steady-state operating conditions are given for a quadratic converter that combines coupled inductor techniques, a voltage doubler cell and diode-capacitor voltage multiplier cell to achieve a high voltage gain [18]. A conventional quadratic boost converter is combined with a coupled-inductor and a voltage multiplier cell [19], which is based on three capacitors and two diodes to obtain a high voltage gain. Unfortunately, the above topology has five different operating conditions in one switching period. When the above topology is used in a switching regulator, the controller will be very difficult to design due to its complex structure.

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In this work, a control strategy is proposed for a converter that combines a quadratic boost converter, a voltage multiplier cell and an output filter [20, 21]. A drawback of using a quadratic boost converter is that the voltage stress on the switching devices is high. The proposed converter increases the output voltage gain and additionally, a significant reduction in the voltage stress on switching devices is obtained [22]. This converter is suitable to be used as interface with low to medium power sources like photovoltaic modules or fuel-cell stacks[23-25]. These renewable energy sources are all series and parallel connections of basic cells that operate at low DC voltage. The resulting modules require, before to be connected to the grid, to step up and regulate their output voltages. Also, require converters with low ripple input current as well as output current, to preserve the useful life of sources and equipment. Electrical models have been developed for the above sources [26, 27], which exhibit a slow response behavior with respect to a high frequency switching converter.

The DC-DC converters, by themselves, cannot provide a regulated voltage without a controller to adjust its operation. Mathematical models that describe their dynamical behavior are required, which can be used in the analysis and controller design under different control strategies. The aim of this paper is to carry out a complete study of the dynamical behavior of a quadratic boost converter with a voltage multiplier cell and then design the corresponding average current-mode controller. The remainder of the paper is organized as follows: In section II, the relationships between voltages, currents and duty cycle are given, as well as the corresponding ripples for the inductor currents and capacitor voltages that allow the proper selection of the converter. The bilinear switched, nonlinear averaged and linear averaged models are derived in section III. In section IV, a step-by-step procedure to design an average current-mode controller is given. The challenge from the control point of view is to select a control strategy such that a design engineer can easily understand and implement the corresponding controller. Experimental results to verify the performance of a switching regulator are shown in section V. Finally, this work concludes in section VI with some final remarks.

II. Analysis Of Steady-State Conditions Of The Converter

There are schemes of voltage multiplier cells (VMC) that can be combined with a quadratic boost converter to step-up the output voltage and to reduce voltage stress on active and passive switching devices. The first one uses a positive voltage multiplier and the second one a negative voltage multiplier. The resulting electric circuits are shown in Fig. 1. Both configurations consist of three inductors, four capacitors, four diodes, and an active switch. The output voltage is represented by V_O and the input voltage by V_{in}. It has been assumed that the voltage source variations are slow enough in comparison to the operation of the converter. The elements of the quadratic boost converter are the inductors L_1 and L_2, and capacitor C_1. The VMC has two capacitors of the same value C_S and diodes D_3 and D_4. The output filter has an inductor L_O and the output capacitor C_O, which is connected in parallel to the output load modeled by R_O. The latter is a typical assumption often used when modeling switching converters [2]. The active switch (MOSFET) is represented by S, passive switches (diodes) are represented by D_1 and D_2; meanwhile, nominal duty cycle is represented by U. The electric circuits that are obtained when active switch S is turned ON and OFF are shown in Fig. 2 and Fig. 3, respectively.

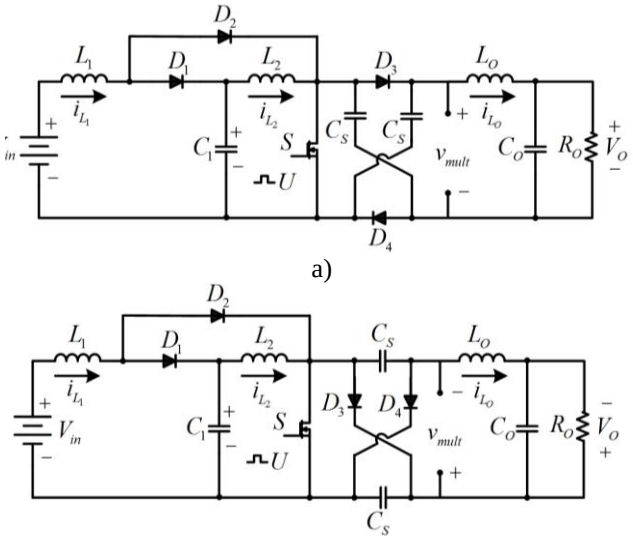

Fig. 1. Quadratic boost converter combined with a voltage multiplier cell: a) positive and b) negative.

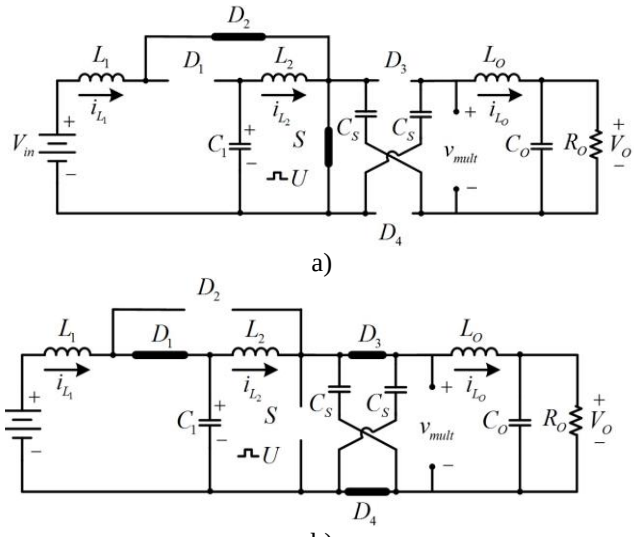

Fig. 2. Operation of quadratic boost converter combined with a positive voltage multiplier cell for: a) S=ON, and b) S=OFF

In this work, it is assumed that proposed converter operates in Continuous Conduction Mode (CCM), that is, the inductors currents never decay to zero. For simplicity, it is assumed that the turn ON and turn OFF transitions of all diodes are synchronized by active switch S. When active switch S is turned ON (Fig. 2(a) and Fig. 3(a)), the inductors L_1 and L_2 store energy and diodes D_1, D_3 and D_4, are not conducing. This produces that capacitors C_S of the VMC will be connected in series; therefore, the voltage V_{mult} is duplicated. When S is OFF (Fig. 2(b) and 3(b)), the stored energy in inductors L_1 and L_2 are used to charge the capacitors C_S. In turn, diodes D_1, D_3 and D_4 are conducing,

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which causes the capacitors of the VMC to be in parallel while they are charging. This series-parallel connection of capacitors of the VMC results in an improvement of the conversion ratio of a conventional quadratic boost converter, as it is shown in Fig. 4.

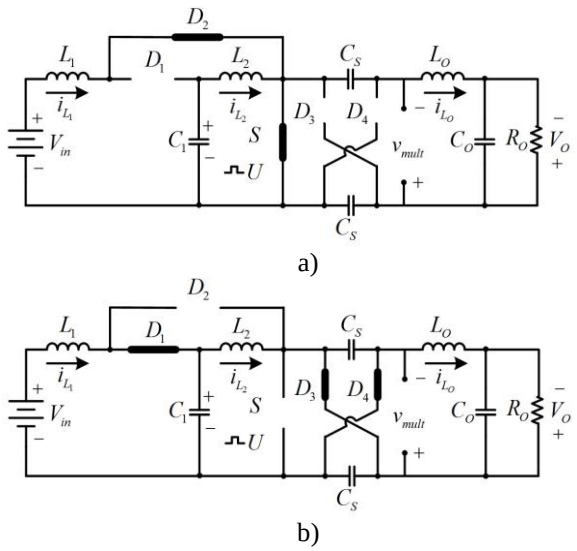

Fig. 3. Operation of quadratic boost converter combined with a negative voltage multiplier cell for: a) *S*=ON, and b) *S*=OFF

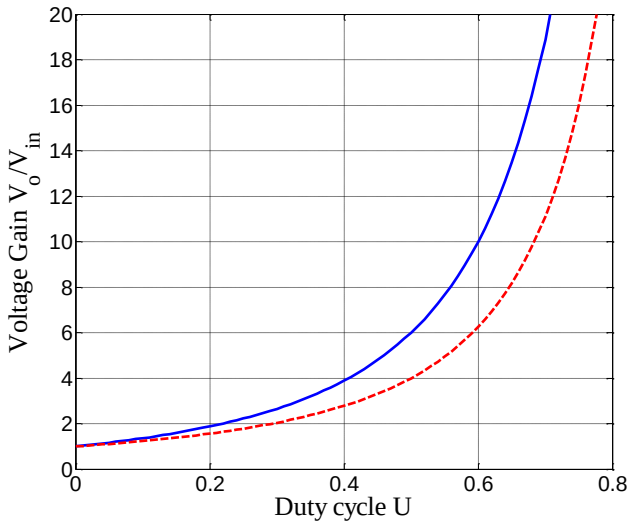

Fig. 4. Comparative plot of voltage gain between: a) Quadratic Boost with voltage multiplier cell converter $V_O/V_{in}=(1+U)/(1-U)^2$ **(top)**, and b) conventional Quadratic Boost converter $V_O/V_{in}=1/(1-U)^2$ **(bottom)**.

By analyzing the resulting electrical circuits when the SW is operating ON and OFF, the average voltage in capacitor C_S is given by:

$$V_{C_S}=\frac{V_{in}}{(1-U)^2}=\frac{V_O}{(1+U)}, \tag{1a}$$

which results in a voltage gain for this converter of

$$\frac{V_O}{V_{in}}=\frac{(1+U)}{(1-U)^2} \tag{1b}$$

The polarity of the output voltage is inverted when a negative VMC is used. For the operation in CCM, the inductors have to satisfy the following conditions:

$$L_1>R_OU(1-U)^4/2f_{SW}(1+U)^2,\ L_2>R_OU(1-U)^2/2f_{SW}(1+U)^2$$
$$\text{and}\ \ L_O>R_OU(1-U)/2f_{SW}(1+U),$$

where f_{SW} is the switching frequency. The expressions for the inductor currents are:

$$I_{L_1}=\frac{V_{in}(1+U)^2}{R_O(1-U)^4},\ I_{L_2}=\frac{V_{in}(1+U)^2}{R_O(1-U)^3}\ \text{and}\ I_{L_O}=\frac{V_{in}(1+U)}{R_O(1-U)^2}. \tag{2}$$

The theoretical ripples of inductor currents and capacitor voltages are useful because a converter should be designed under certain specifications. The ripple ratio in the inductor current is given by $\varepsilon_{i_L}=(\Delta i_L/2)/I_L$. It is suggested that in the conventional converter a value in the range of 10%-20% be used; meanwhile, for the ripple ratio in the capacitor voltage is $\varepsilon_{v_C}=(\Delta v_C/2)/V_C$ and it is suggested that the ripple ratio be in the range of 1%-2%.

The resulting current ripples of inductors can be computed using the following formulae where the behavior of switching devices has been assumed ideal:

$$\Delta i_{L_1}=\frac{V_{in}U}{f_{SW}L_1},\ \Delta i_{L_2}=\frac{V_{in}U}{f_{SW}L_2(1-U)}\ \text{and}\ \Delta i_{L_O}=\frac{V_{in}U}{f_{SW}L_O(1-U)}, \tag{3}$$

and for the voltage ripple of capacitors by:

$$\Delta v_{C_1}=\frac{V_{in}U\ (1+U)^2}{R_OC_1f_{SW}(1\text{-}U)^3},\ \Delta v_{C_S}=\frac{V_{in}U(1+U)}{R_OC_Sf_{SW}(1\text{-}U)^2},$$
$$\Delta v_{C_O}=\frac{V_{in}U}{8L_OC_Of_{SW}{}^2(1-U)}. \tag{4}$$

When the converter is operating in steady state, the voltage stress on the switching devices can be computed by:

$$V_{S_{STRESS}}=\frac{V_O}{(1+U)},$$
$$V_{D_{1STRESS}}=\frac{(1-U)V_O}{(1+U)},\quad V_{D_{2STRESS}}=\frac{UV_O}{(1+U)}, \tag{5}$$
$$V_{D_{3STRESS}}=\frac{V_O}{(1+U)},\quad V_{D_{4STRESS}}=\frac{V_O}{(1+U)}.$$

It can be noticed that a reduce voltage stress is obtained in comparison to the conventional quadratic boost converter.

III. Modeling Of The Proposed Converter

The behavior of this converter can be described through a linear piecewise model that is obtained by means of state space equations of the resulting electrical trajectories when the active switch and diodes are turned ON and OFF, respectively. The state variables that can be identified are the currents of the three inductors and the voltages of the four capacitors. As result of the use of the same value of capacitance for C_S, the voltage is the same in each one when they are connected in series or parallel; therefore, it can be assumed without loss of generality that the voltages in the capacitors of the VMC can be treated as a single variable. Thus, the resulting model is given by (6), where v_{in} is the input voltage, i_{L_1}, i_{L_2} and i_{L_O} are the inductor currents, v_{C_1} and v_{C_S} are the capacitor voltages, and v_O represent the output voltage. The binary switching function is defined by *q*, which has a value of 1 when the active switch is turned ON and 0 when is turned OFF. The model given in (6)

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is bilinear because it involves the product of control variable and some state variables.

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{i}_{L_O} \\ \dot{v}_{C_1} \\ \dot{v}_{C_S} \\ \dot{v}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-q}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1-q}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1+q}{L_O} & -\frac{1}{L_O} \\ \frac{1-q}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-q}{2C_S} & -\frac{1+q}{2C_S} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_O} & 0 & 0 & -\frac{1}{R_O C_O} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_O} \\ v_{C_1} \\ v_{C_S} \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \quad (6)$$

The average value of q can be represented by u (duty cycle of converter), then the average value of currents and voltages [28, 29] can be obtained and the following model is derived:

$$\begin{bmatrix} \dot{\bar{i}}_{L_1} \\ \dot{\bar{i}}_{L_2} \\ \dot{\bar{i}}_{L_O} \\ \dot{\bar{v}}_{C_1} \\ \dot{\bar{v}}_{C_S} \\ \dot{\bar{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-u}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1-u}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1+u}{L_O} & -\frac{1}{L_O} \\ \frac{1-u}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-u}{2C_S} & -\frac{1+u}{2C_S} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_O} & 0 & 0 & -\frac{1}{R_O C_O} \end{bmatrix} \begin{bmatrix} \bar{i}_{L_1} \\ \bar{i}_{L_2} \\ \bar{i}_{L_O} \\ \bar{v}_{C_1} \\ \bar{v}_{C_S} \\ \bar{v}_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \bar{v}_{in} \quad (7)$$

The linearization of (7) can be carried out to describe the converter behavior to small perturbations around an operating point, as is shown in (8). The inductor currents, capacitor voltages, output voltage, control signal and input voltage are decomposed into two parts. The first part contains the nominal values denoted by upper-case letters and the second part the deviations from the nominal denoted by the superscript ~.

IV. Controller Design Of A Switching Regulator

Due to the diverse applications of DC-DC converters with high voltage gains, the designed controller has to overcome several operating conditions. One of them is the case when the input source has its own dynamical behavior and delivers an output voltage with large variations. Another condition is when output load has large variations; therefore, it is necessary a controller with high performance for fast transient response and good regulation when an unregulated source is used and load variations occur.

$$\begin{bmatrix} \dot{\tilde{i}}_{L_1} \\ \dot{\tilde{i}}_{L_2} \\ \dot{\tilde{i}}_{L_O} \\ \dot{\tilde{v}}_{C_1} \\ \dot{\tilde{v}}_{C_S} \\ \dot{\tilde{v}}_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-U}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1-U}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1+U}{L_O} & -\frac{1}{L_O} \\ \frac{1-U}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-U}{2C_S} & -\frac{1+U}{2C_S} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_O} & 0 & 0 & -\frac{1}{R_O C_O} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L_1} \\ \tilde{i}_{L_2} \\ \tilde{i}_{L_O} \\ \tilde{v}_{C_1} \\ \tilde{v}_{C_S} \\ \tilde{v}_O \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{(1-U)L_1} & \frac{1}{L_1} \\ \frac{V_{in}}{(1-U)^2 L_2} & 0 \\ \frac{V_{in}}{(1-U)^2 L_O} & 0 \\ -\frac{(1+U)^2 V_{in}}{(1-U)^4 R_O C_1} & 0 \\ -\frac{(1+U)V_{in}}{(1-U)^3 R_O C_S} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{u} \\ \tilde{v}_{in} \end{bmatrix} \quad (8)$$

There are two approaches widely used to control switching converters: voltage-mode and current-mode. Current-mode has many advantages over voltage-mode control: (a) a faster transient response, (b) easier-to-design control loop, and (c) over-current protection within one switching cycle. The latter will be selected for the above advantages. For control purposes, it is important to select the appropriate variables from the point of view of performance and implementation. This converter has three inductor currents and three capacitor voltages that can be used for feedback; however, it is shown in this paper that the

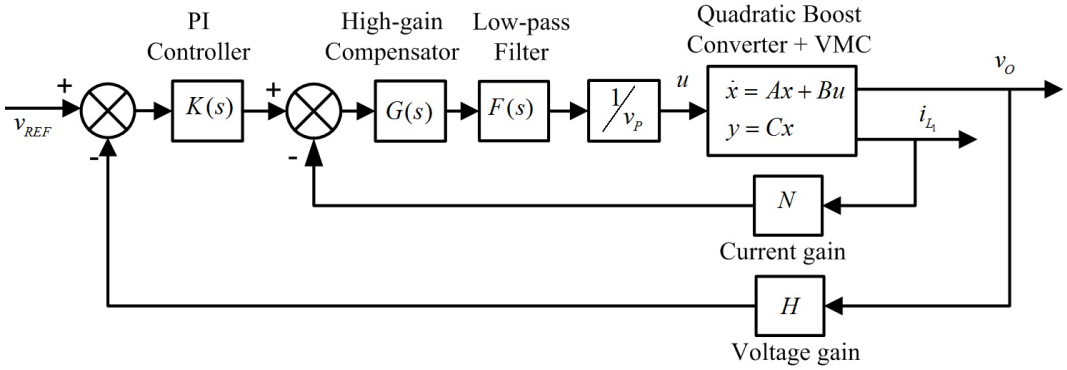

Fig. 5. Switching regulator scheme using a quadratic boost converter combined with a voltage multiplier cell.

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current of first stage inductor together with the output voltage should be selected to successfully implement a controller.

An average current-mode control scheme [30], is shown in Fig. 5, which consists of two loops. The inner or current loop is designed for fast transient response; meanwhile, the outer or voltage loop is implemented for voltage regulation purposes. In this scheme, *H* represents the voltage sensor gain, V_{REF} is a preset value that represents the desired output voltage and the PI controller is represented by the transfer function *K(s).* Additionally, *N* is the current sensor gain, *G(s)* is a high-gain compensator, *F(s)* is a low-pass filter and finally, V_P is the peak magnitude of the ramp used to generate the control pulses.

The overall controller design procedure for this scheme is based on shaping the voltage loop gain $L_V(s)$, i.e. the product of transfer functions in the outer loop. For robust stability, the following requirements have to be satisfied: (i) for relative stability, the slope at or near cross-over frequency must be not more than -20 dB/dec; (ii) to improve steady-state accuracy, the gain at low frequencies should be high; and (iii) for robust stability, appropriate gain and phase margins are required [31].

Now, an easy-to-use procedure is given to ensure suitable loop gain characteristics of the closed-loop.

A. Current loop

The poles and zeros for the current-mode controller are mainly set from the operating switching frequency of the converter. The high-gain compensator and the low-pass filter are represented by the transfer functions:

$$G(s)=\frac{G_P(s+\omega_z)}{s} \quad \text{and} \quad F(s)=\frac{1}{s/\omega_P+1} \tag{9}$$

respectively, where G_P is the high gain of compensator, ω_Z stands for the location of the zero and ω_P for the location of the filter pole. Notice that transfer functions given in (9) can be implemented using a single operational amplifier as shown in Fig. 6; thus, the corresponding control law $\tilde{u}$ is defined by:

$$\tilde{u}=\frac{1}{V_P}\left(\frac{1}{s/\omega_P+1}\right)\left(\frac{G_P(s+\omega_z)}{s}\right)(\tilde{i}_{REF}-N\tilde{i}_{L_1}). \tag{10}$$

The design procedure is given as follows: the high-gain compensator zero ω_Z should be placed at least a decade below of half of the switching frequency f_{SW}. Practically, the zero can be computed by the relationship $\omega_Z=1/R_FC_{FZ}$ where R_F and C_{FZ} are the resistance and capacitance corresponding to the high-gain compensator circuit. The low-pass filter pole ω_P, on the other hand, should be placed either at half of f_{SW} or above. Using the circuitry of Fig. 6, the pole is computed by $\omega_P=(C_{FZ}+C_{FP})/R_FC_{FZ}C_{FP}$ where C_{FP} is the capacitance in the current loop circuit.

The compensator gain is designed such that the current loop gain has a value close to 10 at frequencies around ω_Z. Using the above criterion, the following expression is obtained for the compensator gain

$$G_P<\frac{5V_PU(1-U)^3R_O}{NV_O(3+U)}. \tag{11}$$

It can be noticed that this inequality depends on the output load; therefore, the gain G_P has to be adjusted for possible changes in the load. A good approximation is to multiply this gain for about 8 to 10 times. The compensator gain is computed by $G_P=R_F/R_1$ by the proper selection of resistances.

B. Voltage loop

Once the current loop has been tuned, the voltage loop gain is now designed. The outer loop provides output voltage regulation using a PI controller. The above will result in a high gain at low frequencies. The transfer function for the PI controller is given by

$$K(s)=K_P\left(1+\frac{1}{T_is}\right), \tag{12}$$

where $K_P=R_{FC}/R_{1C}$ is the proportional gain and T_i the integral time. The resulting reference current for this loop is

$$\tilde{i}_{REF}=K_C\left(1+\frac{1}{T_is}\right)(\tilde{v}_{REF}-H\tilde{v}_O). \tag{13}$$

The proportional gain should be selected such that appropriate gains and phase margins are obtained. An approximation for K_P can be obtained such that the voltage loop gain has a value less than 1 at frequencies above ω_Z

$$K_P<\frac{2N(1+U)}{HR_O(1-U)^2}. \tag{14}$$

Finally, the integral time is computed by $T_i=R_{FC}C_{FC}$ where R_{FC} and C_{FC} are the resistance and capacitance values of the PI controller such that $1/T_i$ should be placed at least one decade below f_{SW}.

The expressions (11) and (14) provide a first approximation to the current and voltage gains. An iterative procedure has to be followed for the proper tuning of the controllers to obtain appropriate gain and phase margins to guarantee robust stability, which has to be verified by experimental measurements.

V. Experimental Results

A switching regulator based on a quadratic-boost converter with a VMC has been implemented experimentally to validate the above procedure, see Fig. 6. The operating values for the converter are: input voltage V_{in} of 24 V, output voltage V_O of 220 V and duty cycle of U = 0.594. The steady-state average current for the first inductor is 16.3 A, for the second inductor is 6.43 A and for third inductor is 1.36 A. The nominal load is 161 Ω, which results in an output power of 300 W. The operating switching frequency of the converter is 100 kHz. The parameters of proposed converter are shown in Table 1.

The selected nominal values of the capacitors result in the following voltage ripples $\varepsilon_{v_{C1}}=1.89\%$, $\varepsilon_{v_{CS}}=0.63\%$ and $\varepsilon_{v_{CO}}=0.41\%$, and the current ripples of the inductors by $\varepsilon_{i_{L1}}=8.56\%$, $\varepsilon_{i_{L2}}=12\%$ and $\varepsilon_{i_{LO}}=10\%$. The voltage stress on the active switch is 138 V. The current transducer LA50-P by LEM has been used for sensing the first inductor current.

The transfer functions of selected variables proposed for control purposes are computed using the values of converter parameters. When the values of the converter are substituted in (8), the corresponding transfer functions between variables of interest are obtained.

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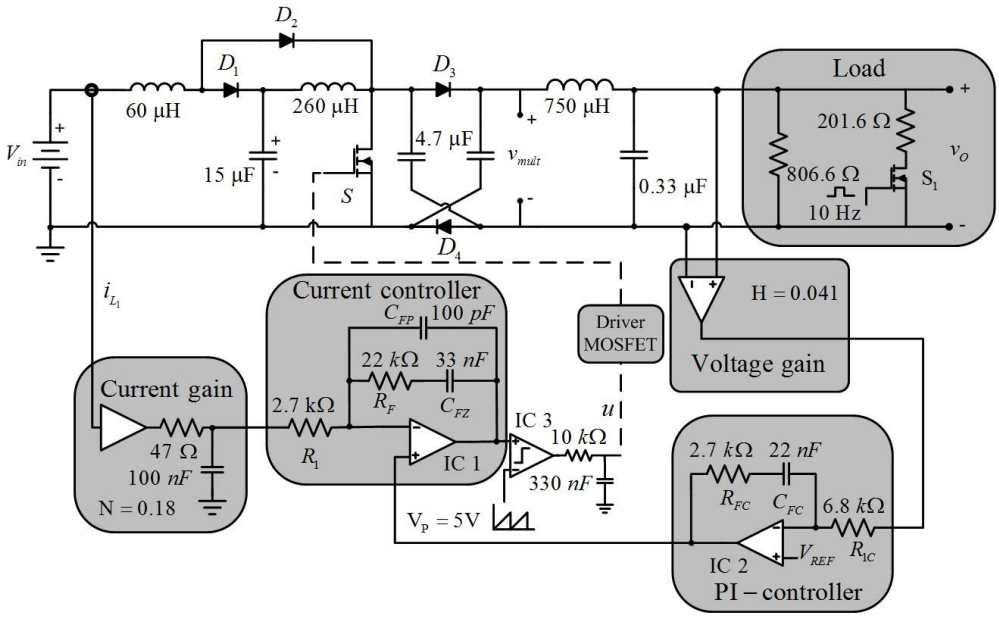

Fig. 6. Experimental prototype implemented in the laboratory.

TABLE 1

PARAMETERS OF SWITCHING REGULATOR	
Inductor L_1	60 µH
Inductor L_2	260 µH
Inductor L_O	750 µH
Capacitor C_1	15 µF
Capacitors C_S	4.7 µF
Output capacitor C_O	0.33 µF
Nominal load resistance R_O	161 Ω
Diodes D_1 and D_2	(Schottky) DSA120C150QB
Diodes D_3 and D_4	40EPF08
MOSFETs S and S_1	IRF4668
OpAmp IC1 and IC2	TL81
Comparator IC3	LM 311
Current sensor	LA50P

The transfer function $\tilde{v}_O(s)/\tilde{u}(s)$ is given by (15a), with poles located at {- 8.602 × 10^3 ± j65.58× 10^3, -81.91 ± j22.8× 10^3, -707.6 ± 5.027× 10^3}. This a six-order converter with three high-resonances peaks, which depend on the parameters of the converter. Some of the coefficients of numerator have negative signs; therefore, there are zeros located in the right-hand side (RHS) of s-plane. This transfer function exhibits a non-minimum phase behavior. The zeros are located at {-474.2 ± j24.55× 10^3, 4.451× 10^3 ± j13.21× 10^3}. Stability and good performance are very difficult to achieve with a single control loop due to two RHS zeros. When the transfer function $\tilde{i}_{L_1}(s)/u(s)$ is computed results in (15b), which has zeros located at {-8.616× 10^3± j65.53× 10^3, -2.238× 10^3 ± j23.96× 10^3, -3.063× 10^3}. This transfer function has a minimum phase behavior. The computation of the transfer function $\tilde{i}_{L_2}(s)/\tilde{u}(s)$results in (15c), where negative coefficients appear in the numerator polynomial; therefore, this transfer function exhibits a non-minimum phase behavior. The first inductor current is a good selection for feedback and it can also be used for over-current protection.

A controller for the switching regulator was designed following the guidelines of previous section. Using the expression given in (11), the gain G_P of the compensator should be 1.12; however, this gain should take in consideration the possible changes in the load. Thus, resistances R_F and R_1 have been selected to provide a gain of 8.15. The gain of compensator K_P should satisfy the inequality given in (14), which for the converter results in 0.499. The selected circuit elements results in a gain of 0.40.

Open and closed-loop experimental test were performed at the nominal values, then step changes are applied in the load. Load changes are generated through the switch S_1 and have a

$$\frac{\tilde{v}_O}{\tilde{u}} = \frac{560.34\times10^9 s^4 - 4.47\times10^{15} s^3 + 442.17\times10^{18} s^2 - 2.91\times10^{24} s + 65.73\times10^{27}}{s^6 + 18.82\times10^3 s^5 + 4.92\times10^9 s^4 + 16.48\times10^{12} s^3 + 2.27\times10^{18} s^2 + 3.26\times10^{21} s + 55.01\times10^{24}} \quad (15a)$$

$$\frac{\tilde{i}_{L_1}}{\tilde{u}} = \frac{951.54\times10^3 s^5 + 23.87\times10^9 s^4 + 4.90\times10^{15} s^3 + 43.31\times10^{18} s^2 + 2.52\times10^{24} s + 7.47\times10^{27}}{s^6 + 18.82\times10^3 s^5 + 4.92\times10^9 s^4 + 16.48\times10^{12} s^3 + 2.27\times10^{18} s^2 + 3.26\times10^{21} s + 55.01\times10^{24}} \quad (15b)$$

$$\frac{\tilde{i}_{L_2}}{\tilde{u}} = \frac{533.40\times10^3 s^5 + 7.95\times10^9 s^4 + 2.56\times10^{15} s^3 - 979.84\times10^{15} s^2 + 8.93\times10^{21} s + 2.42\times10^{27}}{s^6 + 18.82\times10^3 s^5 + 4.92\times10^9 s^4 + 16.48\times10^{12} s^3 + 2.27\times10^{18} s^2 + 3.26\times10^{21} s + 55.01\times10^{24}} \quad (15c)$$

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range from 161 Ω to 806 Ω, that is, from full to 20% of load at a frequency of 10 Hz.

A. *Open loop test*

The currents flowing through i_{L_1} and i_{L_O} are shown in Fig. 7. As it can be seen, both currents have a DC component with small ripple, which depends on the inductance value. This ripple can be reduced when the corresponding inductances are increased.

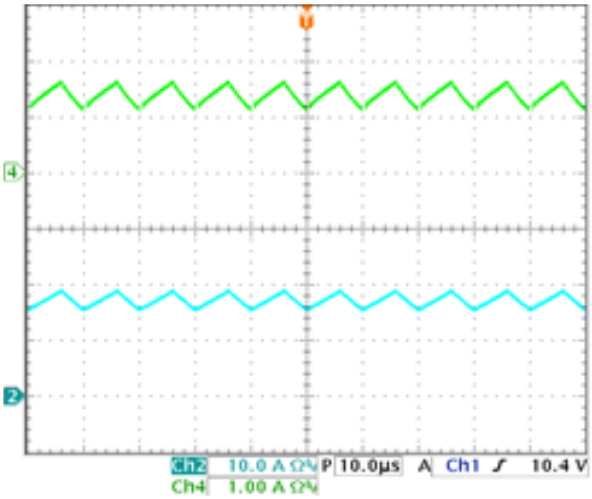

Fig. 7. Waveforms of the inductor currents. **(From top to bottom)** Current flowing through i_{L_1} (10 A/div) and current flowing through i_{L_O} (1 A/div) (Time: 10 µ s/div).

The multiplying effect due to diodes D_3 and D_4 over capacitors C_S will produce the series-parallel connection as shown in Fig. 8. The VMC output voltage V_{mult} that is applied to the output filter changes from 135 V to 260 V.

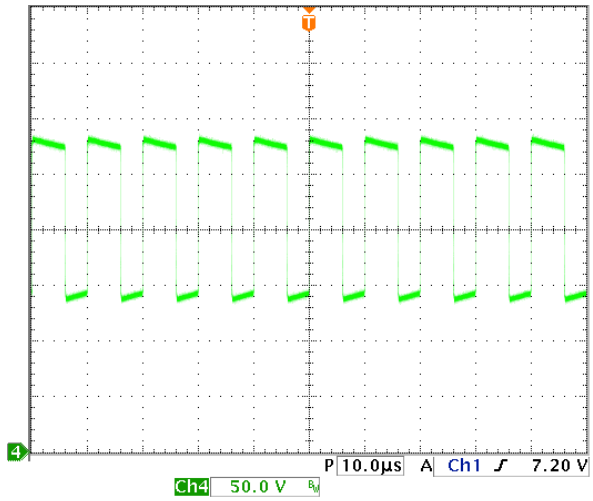

Fig. 8. Voltage applied to the output filter. Voltage V_{mult} (50 V/div) (Time: 10 µ s/div).

The response of the proposed converter when step changes are applied to the load is shown in Fig. 9. The resulting output voltage changes from 220 V to 250 V with small peaks in the transitions. The variation of the output voltage is about 30 V. The effect that the load variations have in the performance of the converter is clear.

B. *Closed-loop test*

The experimental frequency response for the voltage loop gain is shown in Fig. 10. The plot was obtained at nominal load using the Frequency Response Analyzer 300 from AP Instruments. The voltage loop gain has a gain margin of 30 dB, a phase margin of 90 degrees and bandwith of 450 Hz; thus, robut stability is guaranteed. Furthermore, the voltage loop gain is dominated by the PI controller and exhibits high gain at low frequency, which is needed for voltage regulation.

The resulting output voltage of the regulator at nominal conditions is depicted in Fig. 11 for an input voltage of 24 V and an output voltage of 220 V.

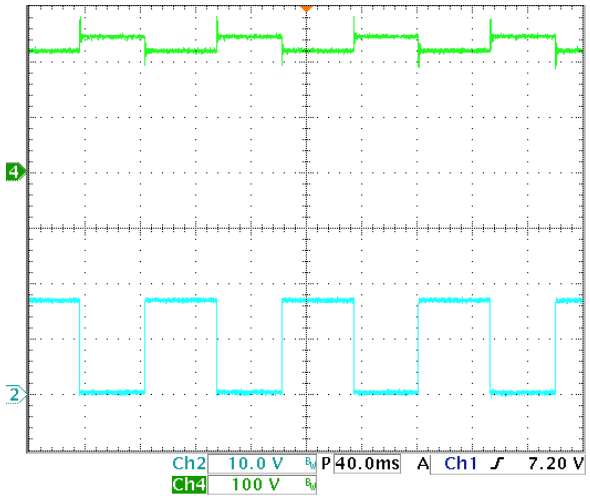

Fig. 9. Time response in open loop of the proposed converter when step changes are applied to the load. **(From top to bottom)** Output voltage V_O (100 V/div) and gate voltage of MOSFET S_1 (10 V/div) (Time: 40 ms/div).

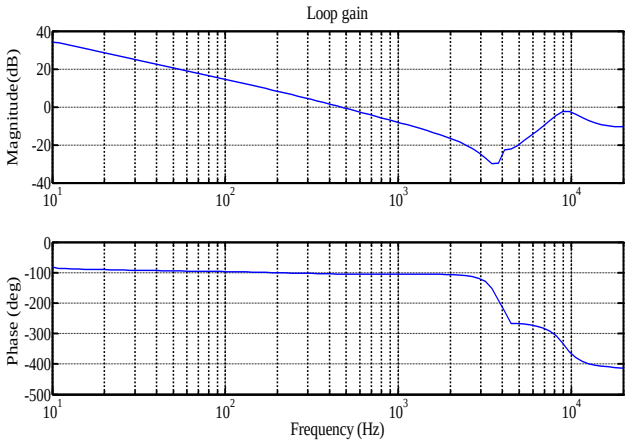

Fig. 10. Experimental frequency response of voltage loop gain at nominal load: (**From top to bottom**) magnitude (y-axis: 20 dB/div), and phase (y-axis: 100 deg/div).

The output voltage regulation is shown in the Fig. 12 when load step changes are applied. As it can be seen, the output voltage remains constant despite changes from full load to 20% load.

The efficiency of regulator was measured and depicted in Fig. 13. The efficiency is about 88% at low power and above 82% at nominal power. The losses are mainly due to the switching devices[32]. It is clear that the development of devices with new semiconductor materials will result in better efficiencies for the converters.

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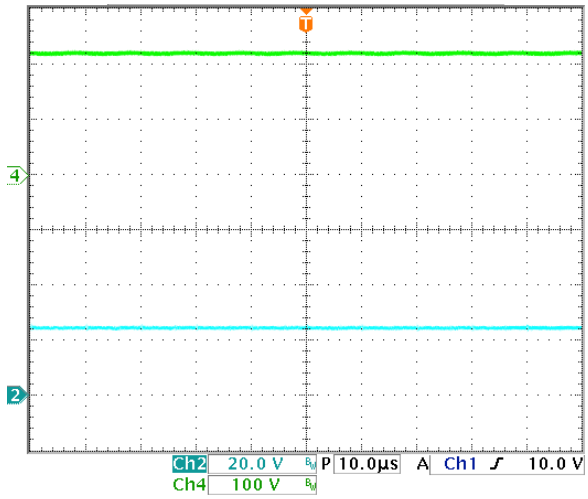


Fig. 11. Closed-loop time response for the output voltage of the switching regulator: **(From top to bottom)** Output voltage v_O (y axis: 100 V/div), and input voltage v_{in} (y-axis: 20 V/div), (x-axis: time 10 µs/div).

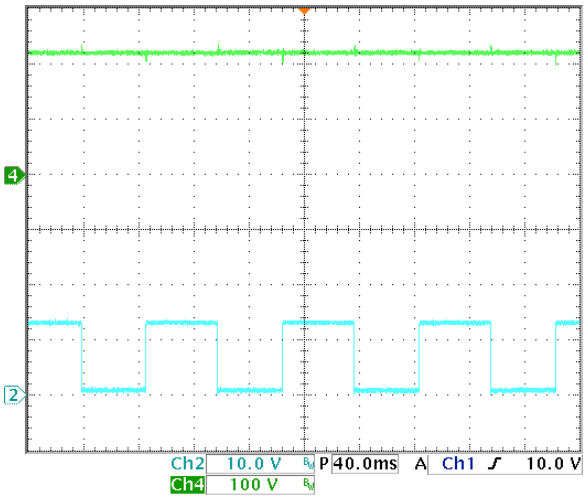


Fig. 12. Closed-loop time response of output voltage for step changes in the load: (**From top to bottom**) Output voltage v_O (y axis: 100 V/div), and trigger voltage $v_{G_{S1}}$ (y-axis: 10 V/div), (x-axis: time 40 ms/div).

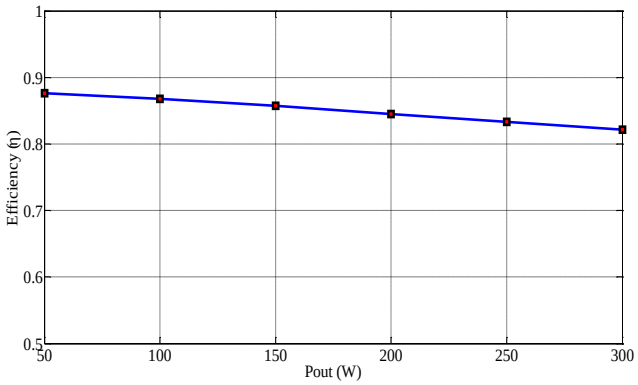
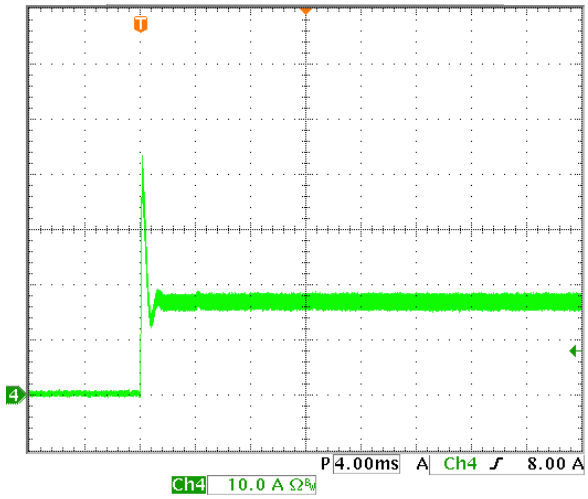
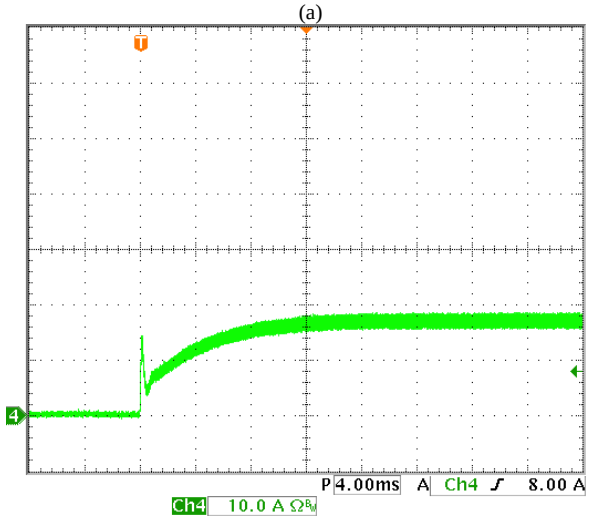


Fig. 13. Efficiency of switching regulator using a quadratic boost converter with voltage multiplier cell.

The converter is tested in open loop at the start-up, this condition being important because the storage elements need to be charged to the nominal operation. The inrush current increases up to 60 A, that is, it exhibits a 233% of overshoot, which is very high and may damage the switching devices. Now, the controller is enabled and the input current is measured, see Fig. 14(a). The inrush current is about 44 A, that is, 169% overshoot. It is important to add a circuit to mitigate the inrush current [24]. A simple solution is to use a RC network in the input of the reference voltage. A resistance of 10 kΩ and a capacitance of 0.33 µF are selected for the RC network, which has a time constant of 3.3 ms. The switching regulator is tested using the RC network, see Fig. 14 (b). The input current increases slowly until it arrives to the nominal operation. It is clear that inrush current of switching regulator remains small; however, a small peak appears at the beginning.



(a)



(b)

Fig. 14. Input current i_{in} of the switching regulator at the start: (a) without the RC network and (b) with the RC network. (y-axis: 10 A/div), (x-axis: time 4 ms/div).

VI. Concluding Remarks

The converter discussed in the paper has the advantage of high voltage gain with non-pulsating input and output currents; therefore, it is very attractive for many applications. This converter uses a voltage multiplier cell, which increases the voltage gain and reduces the voltage stress that appears in the switching devices. When the positive voltage multiplier cell is used, the voltage gain is $V_O / V_{in} = (1+U)/(1-U)^2$; however,

when the negative voltage multiplier cell is used, the voltage gain is $V_O / V_{in} = -(1+U)/(1-U)^2$. The operation of these cells is very similar. It can be noticed that due to the high gains, these converters are highly sensitive to changes in the duty cycle. The formulae for the inductor and capacitor ripples are given such that a converter can be designed to operate under certain specifications. The bilinear switched, nonlinear averaged and linear averaged models are obtained to describe the dynamical behavior of proposed converter. Current-mode control has been selected where the inner loop is used for fast response and the outer loop for voltage regulation. Furthermore, a simple and well-defined procedure for the selection of the controller parameters is given, which ensures robust stability and output voltage regulation. An improper design will result in instability and bad performance. The critical parameters of the design are the gains of controllers. The simplicity of this approach is of significant value in which the analytic results can be used to make design choices and tradeoffs between the inner and outer loops. A controller designed for a switching regulator delivering an output power of 300 W shows good voltage regulation despite of step changes in the load.

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